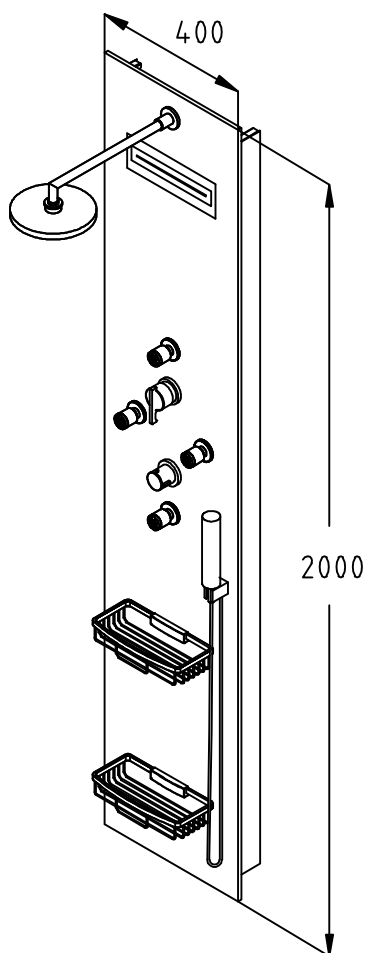
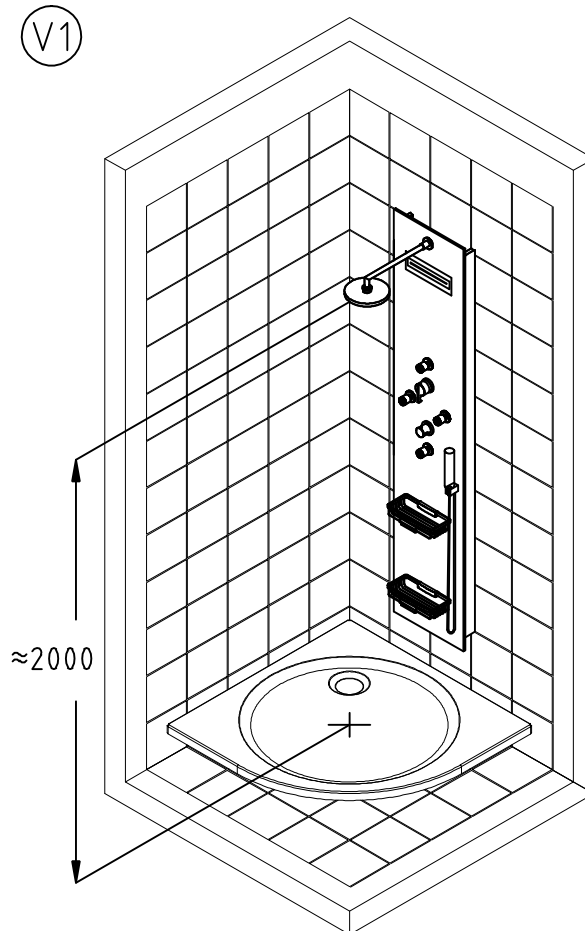


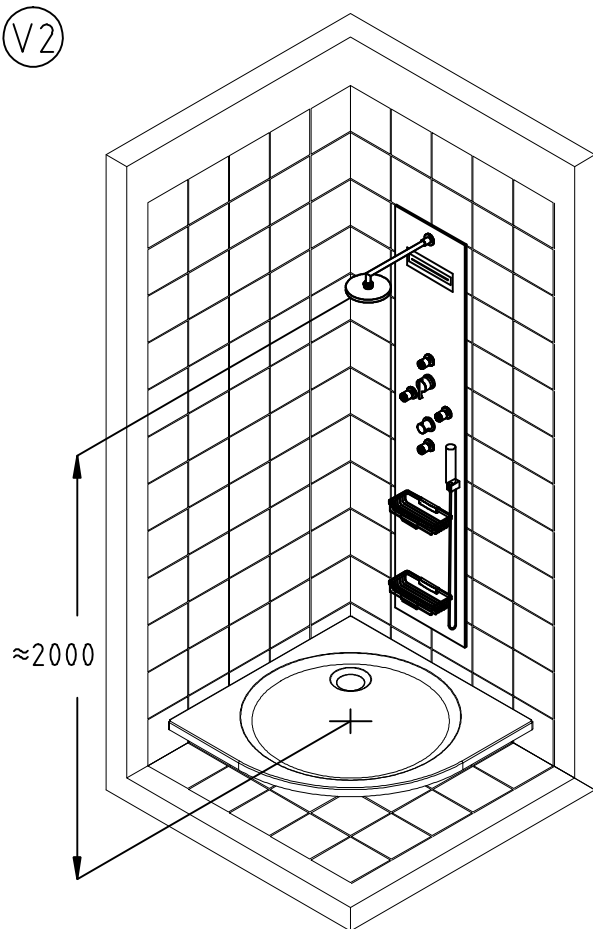
V1 V2 V3



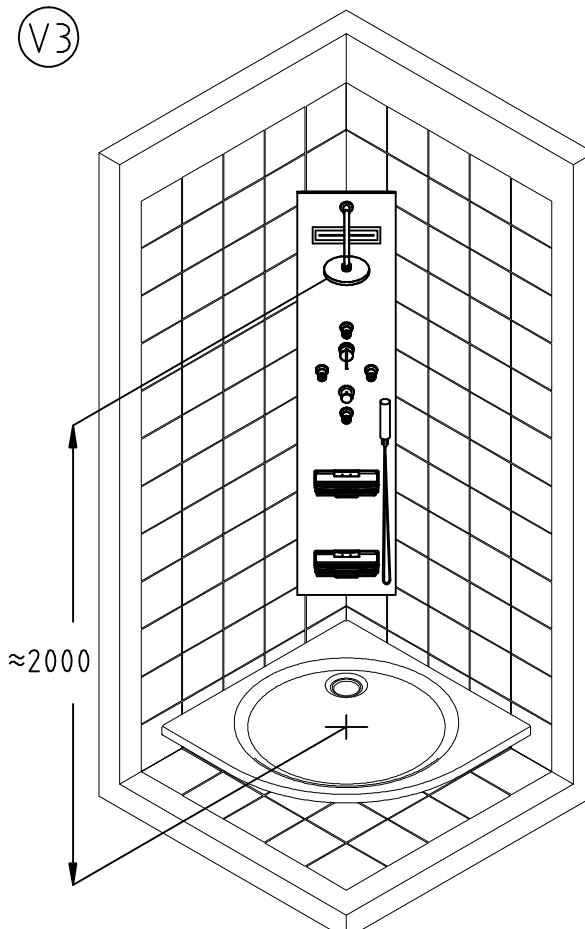
V1

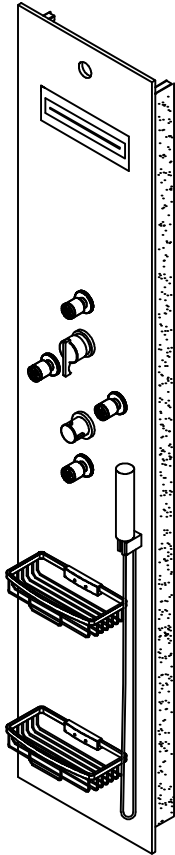
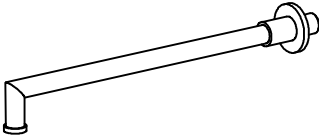
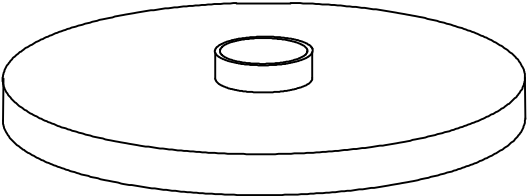
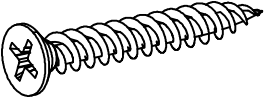
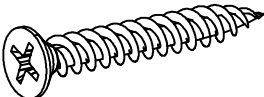
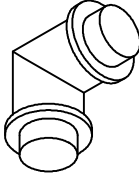
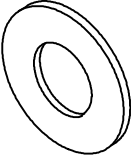
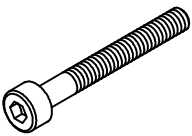


V2

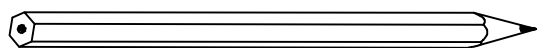


V3

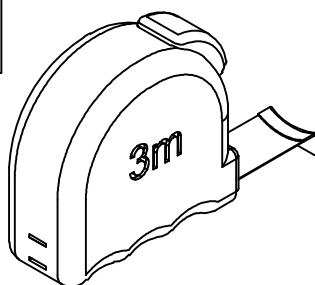


A  V1 V2 V3 1x	B V1 V2 V3  1x	C V1 V2 V3  1x
H V1 V2  6x	I V3  8x	J V1 V2 V3  2x
K V1 V2 V3  1x	L V1 V2 V3  1x	M V1 V3  2x
80620 2/9		

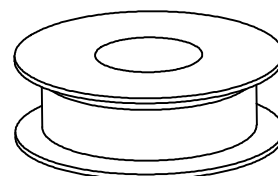
N



O

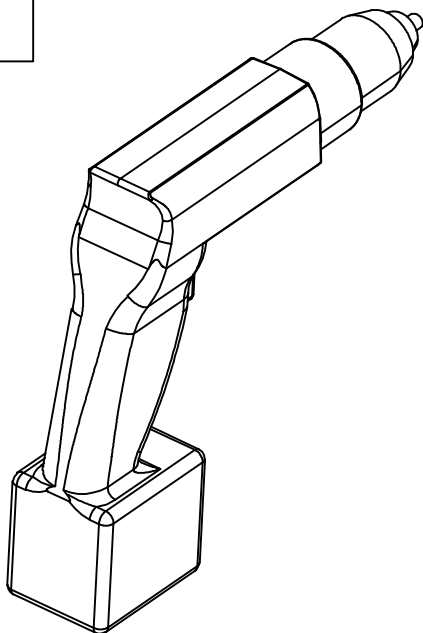


P



TEFLON

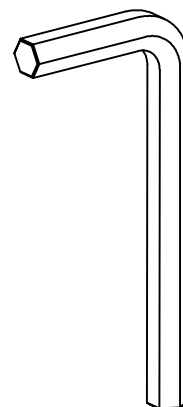
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R

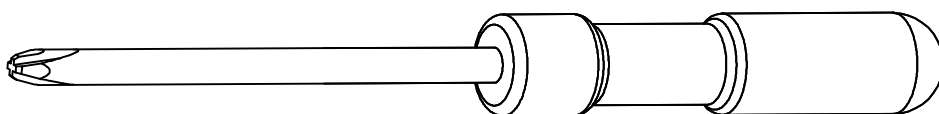


S

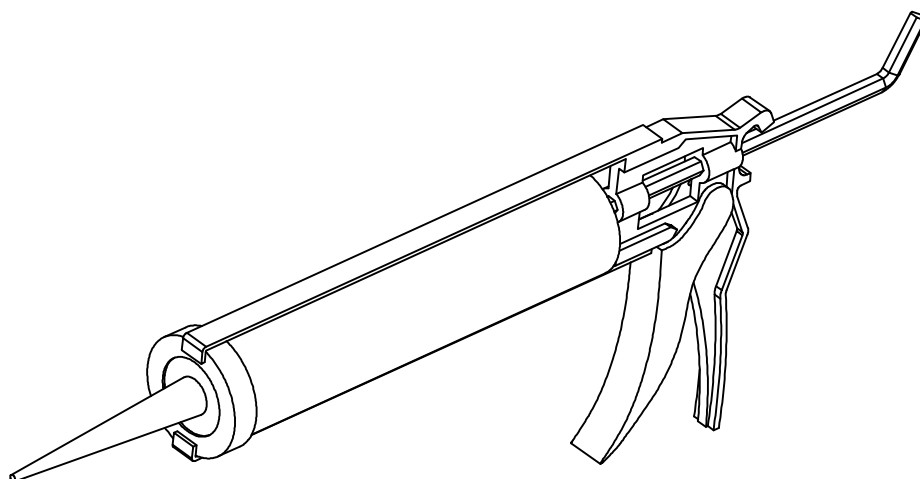


IMBUS 2.5

T

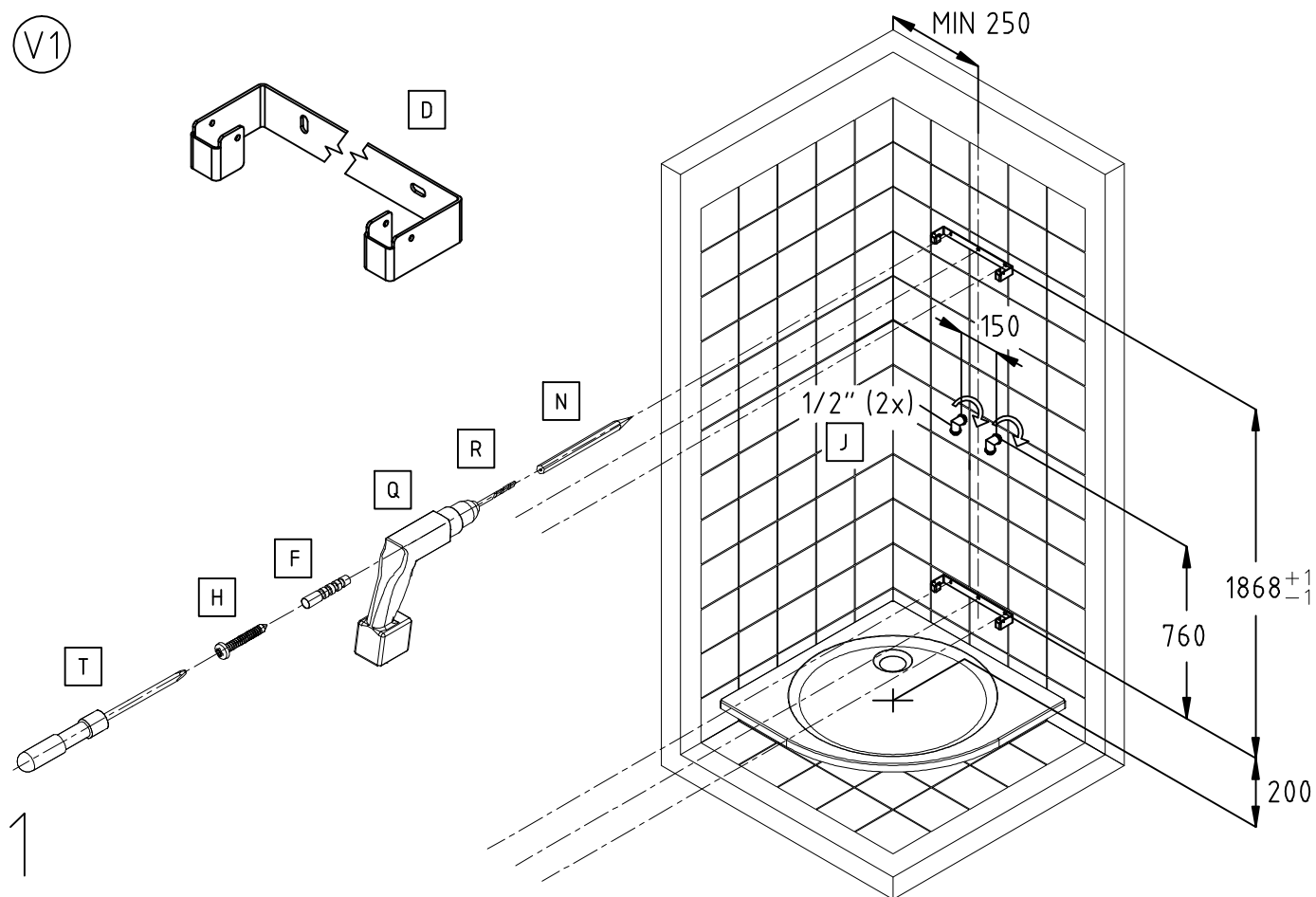


U

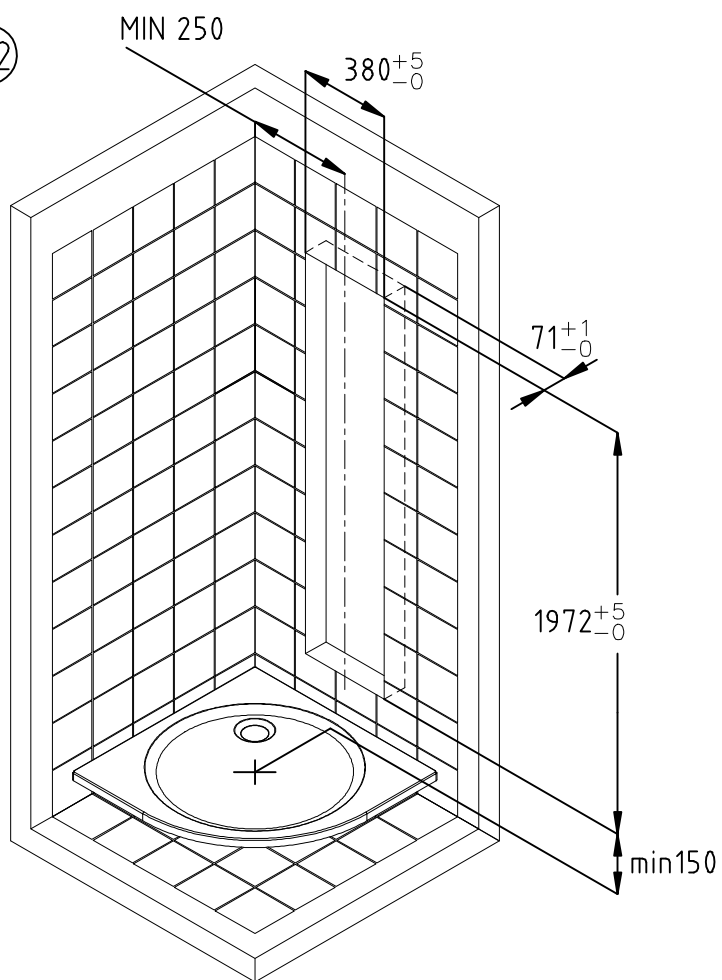


SILIKON

V1



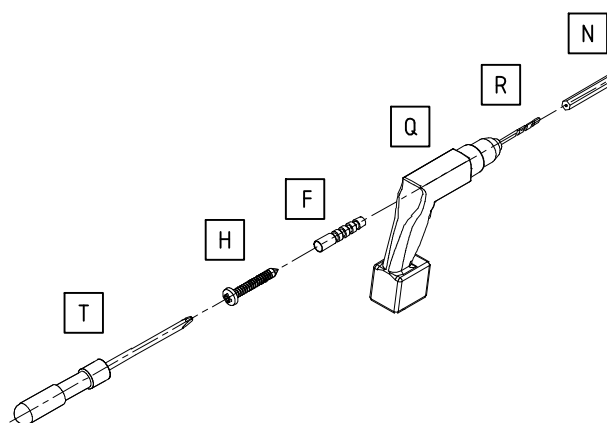
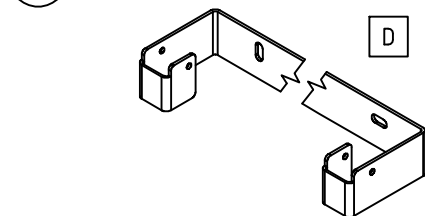
V2



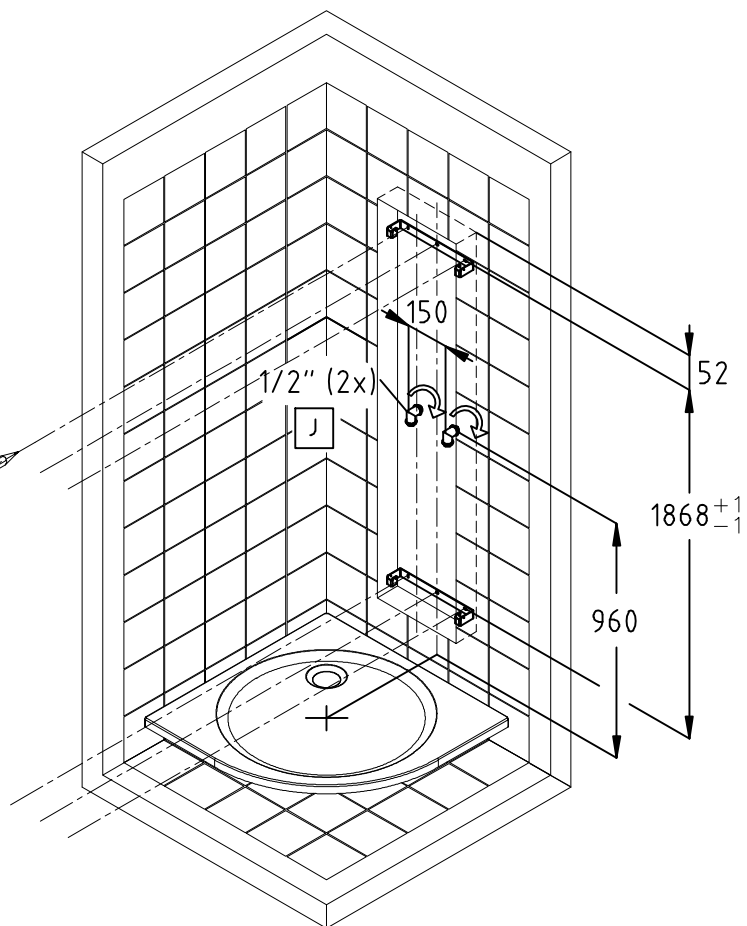
80620

4 / 9

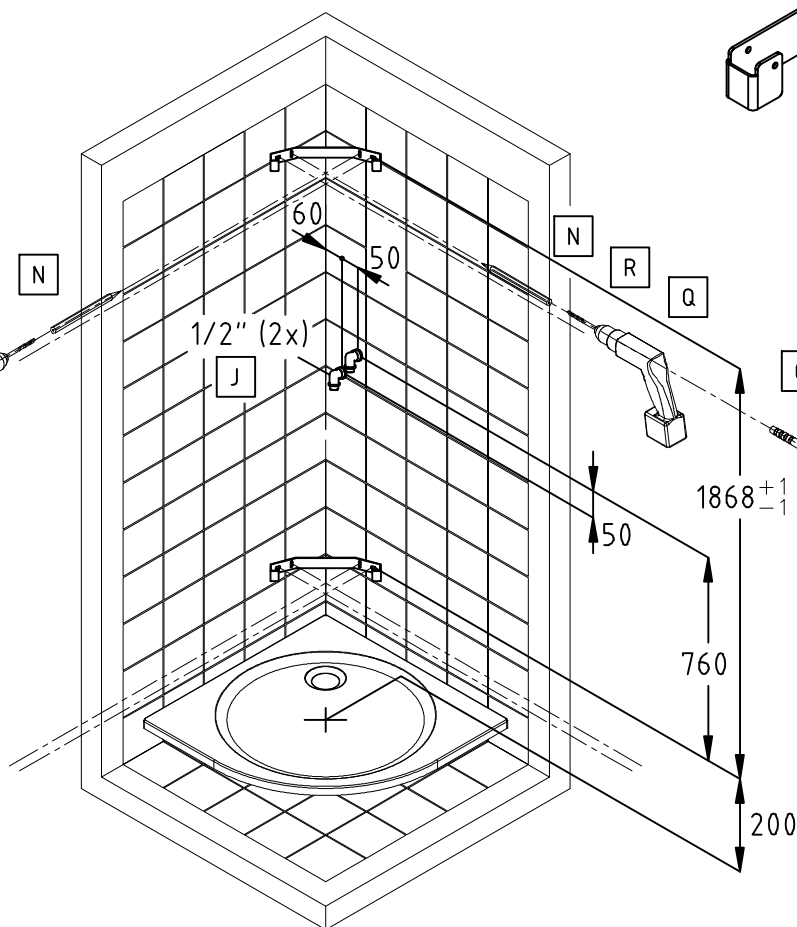
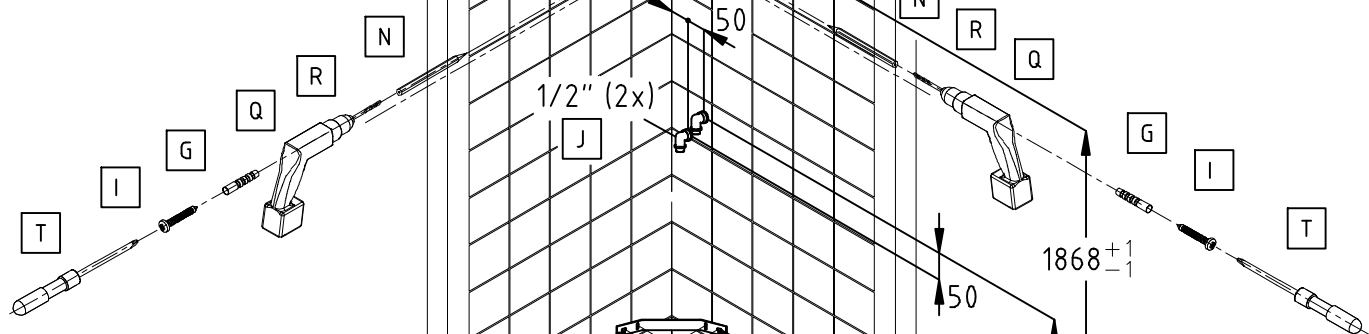
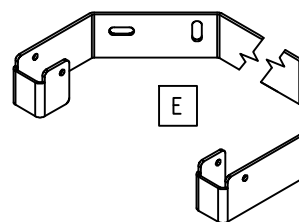
V2



3



V3

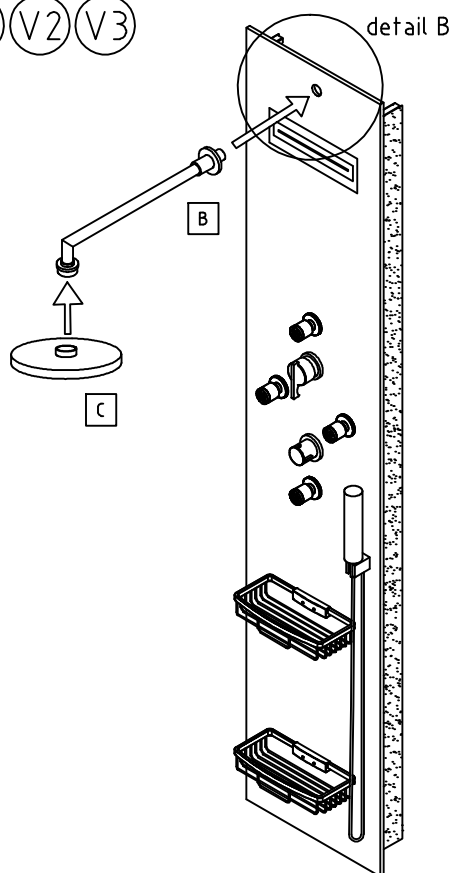


4

80620

5/9

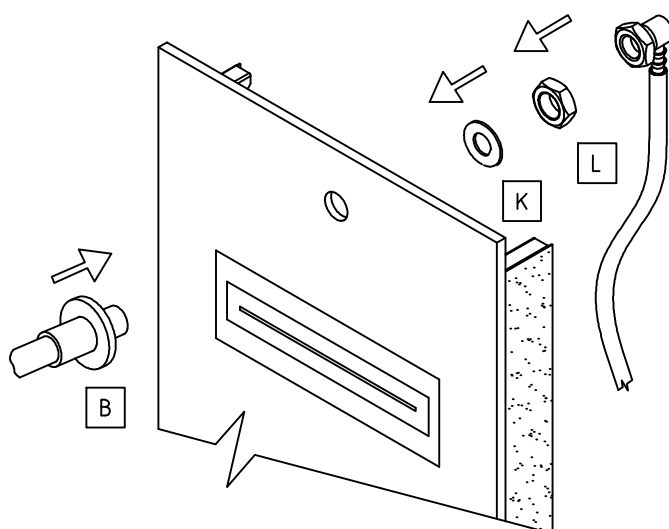
V1 V2 V3



5

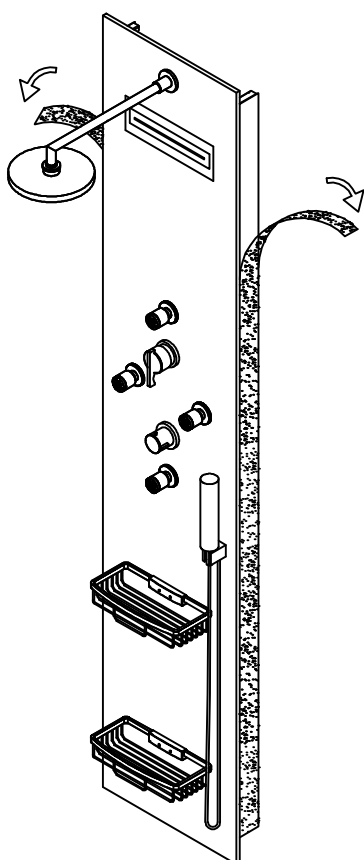
V1 V2 V3

detail B



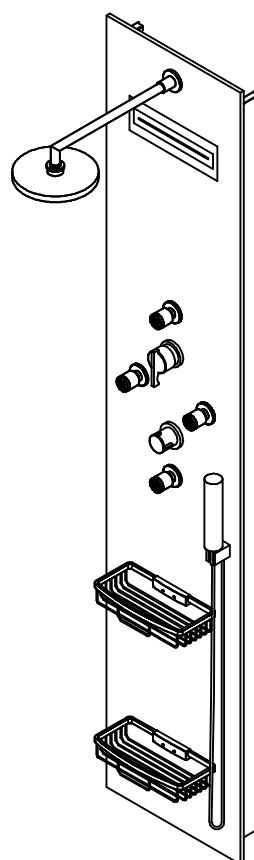
6

V1 V2 V3



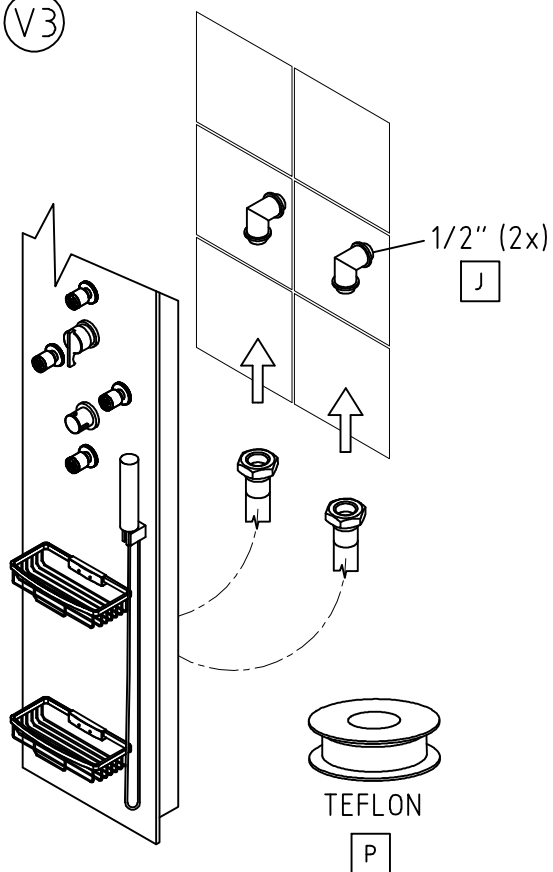
7

V1 V2 V3



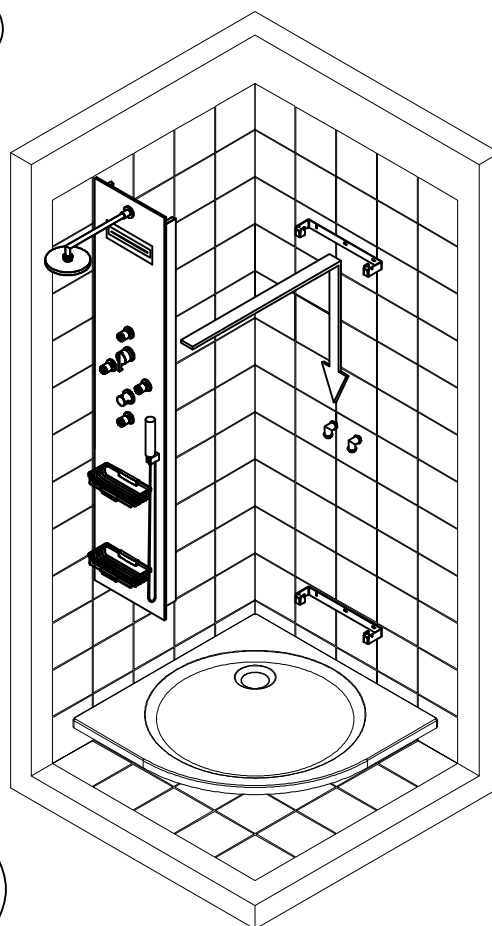
8

V1 V2 V3



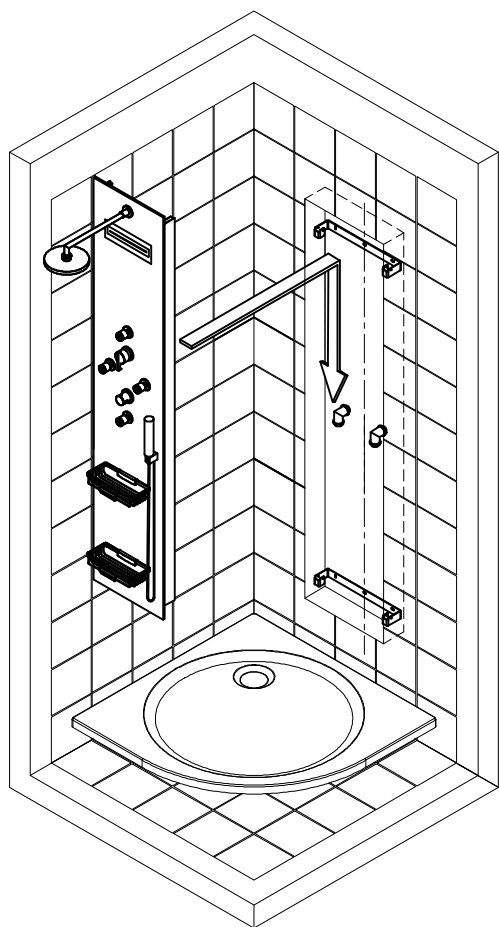
9

V1



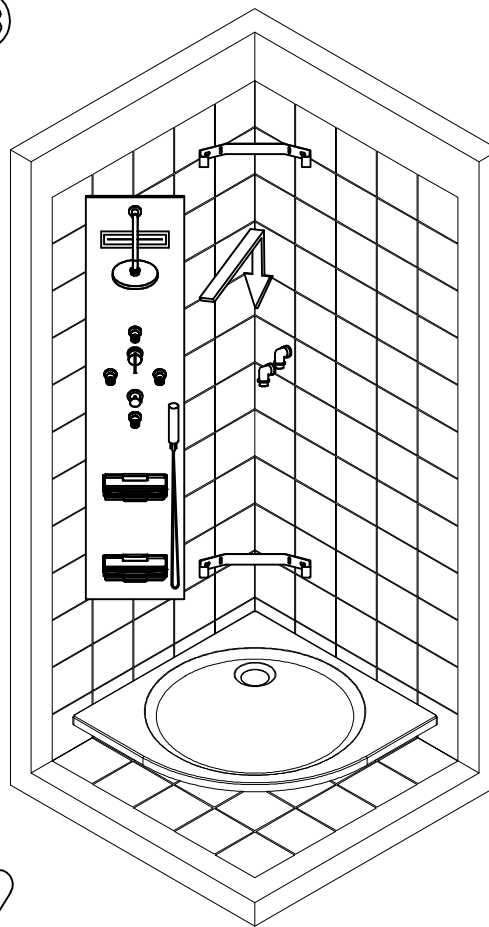
10

V2



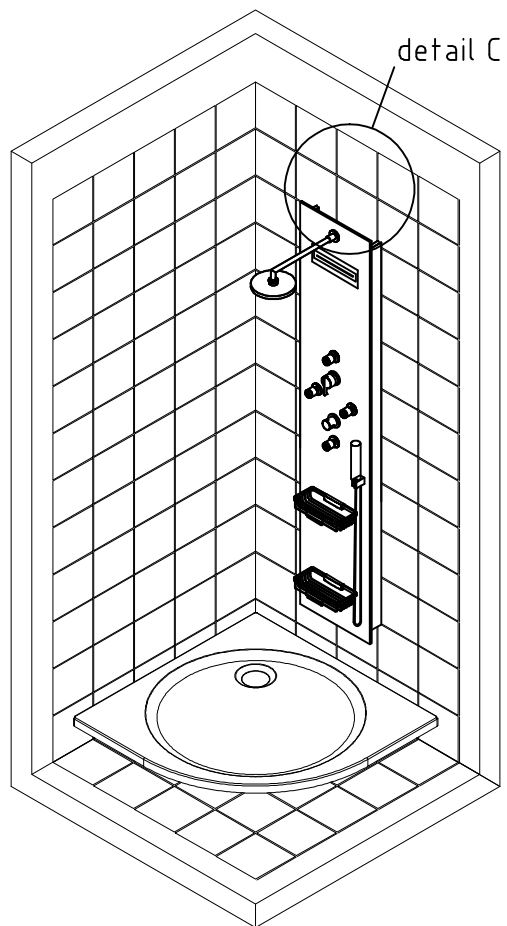
11

V3



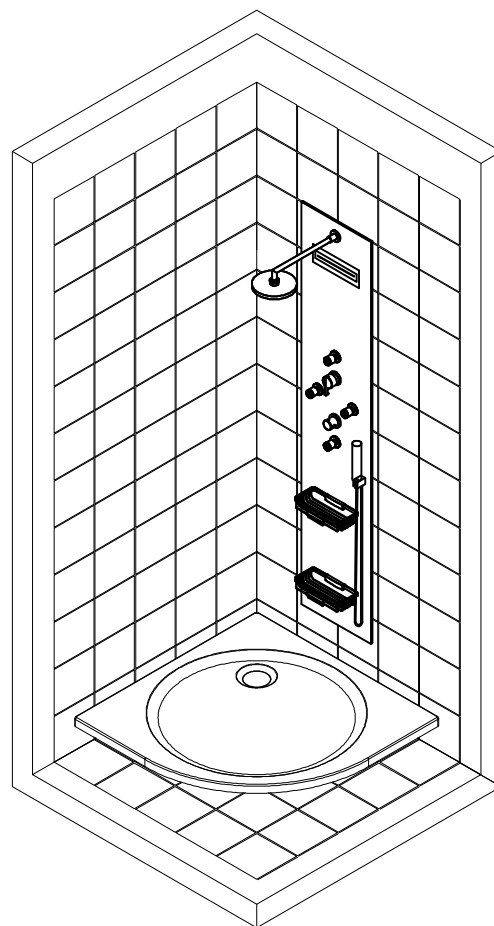
12

V1



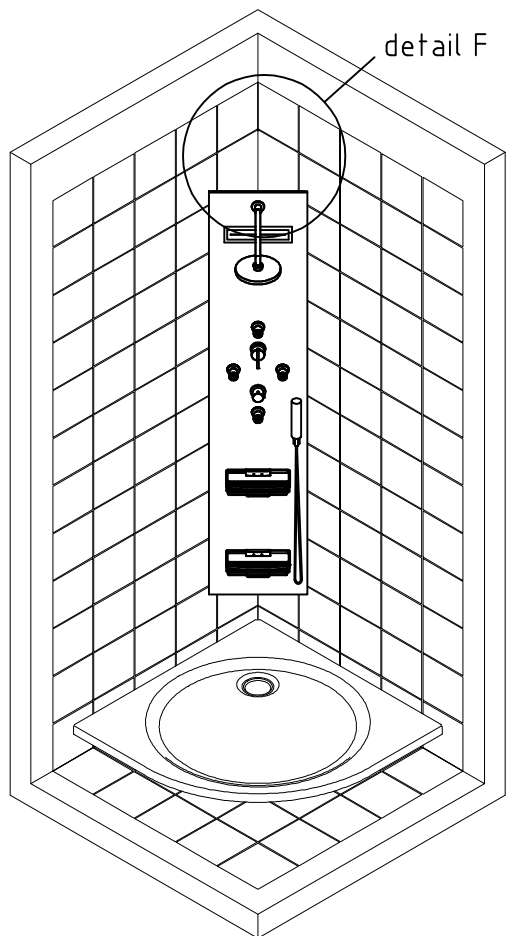
13

V2



14

V3



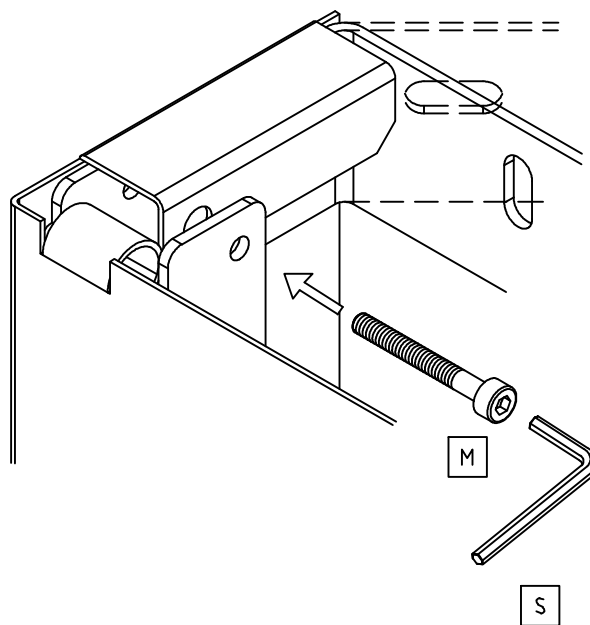
15

V1

detail C

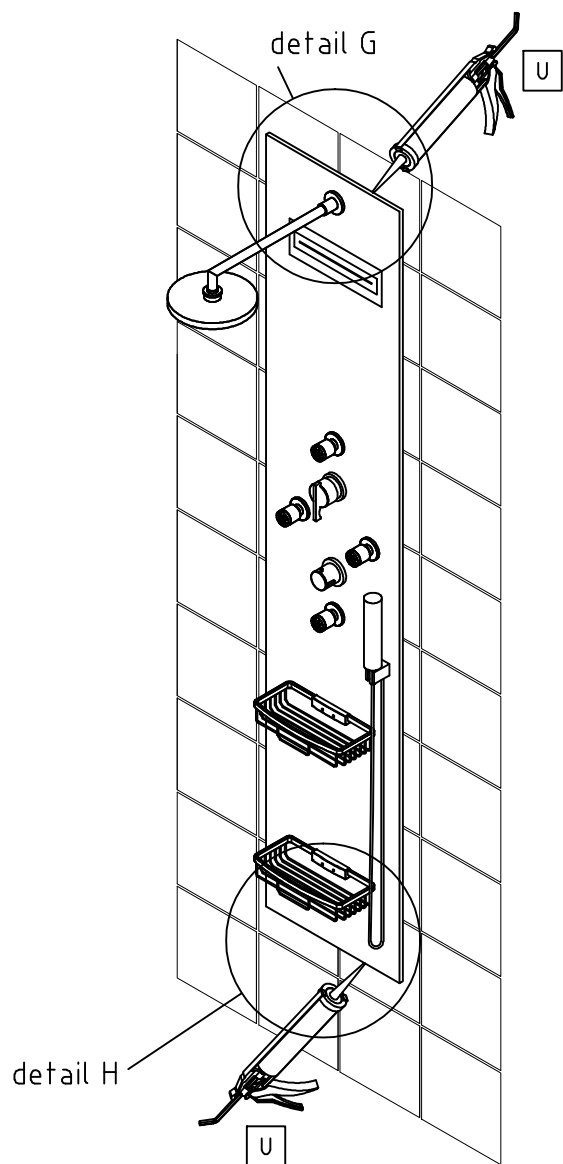
V3

detail F



16

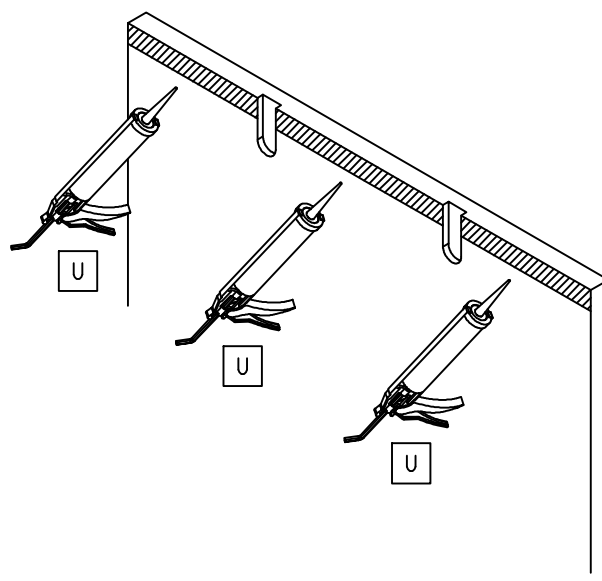
V2



17

V2

detail G
detail H



18