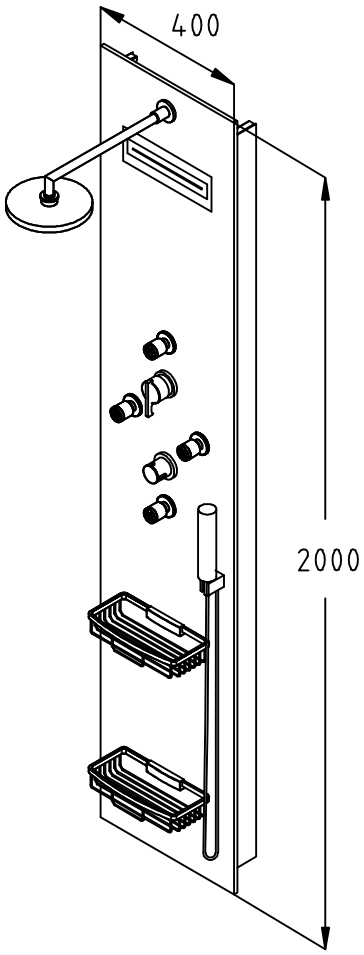
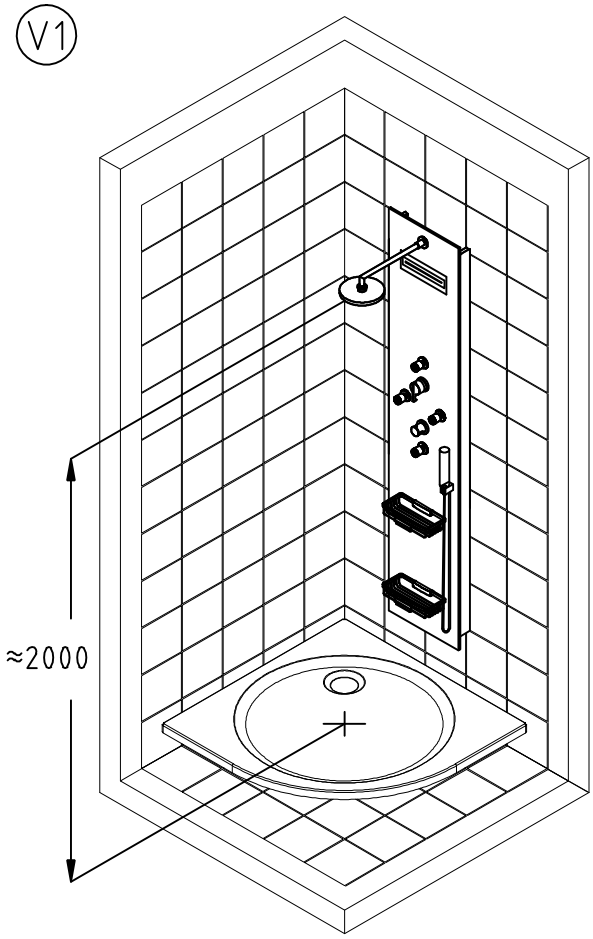
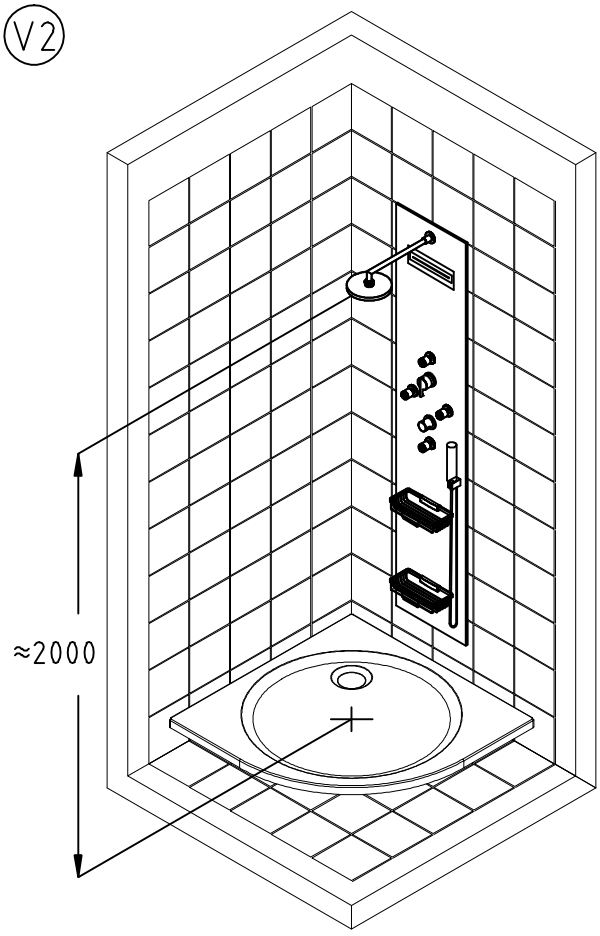
V1 V2 V3



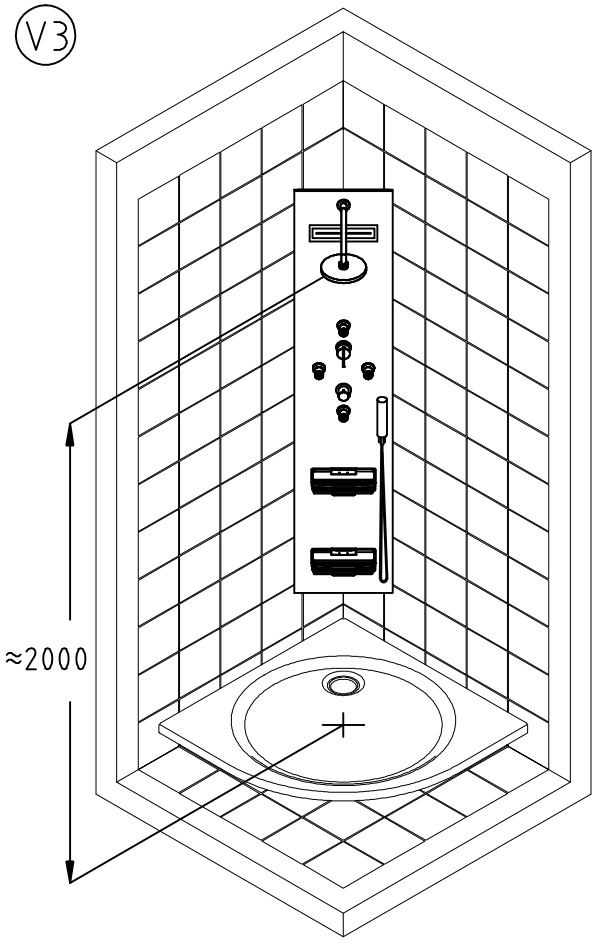
V1



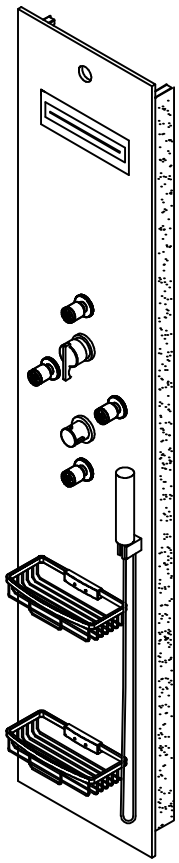
V2



V3



A

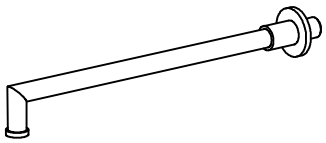


V1 V2 V3

1x

B

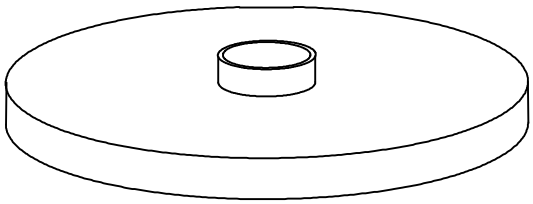
V1 V2 V3



1x

C

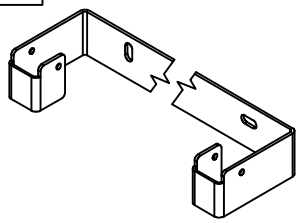
V1 V2 V3



1x

D

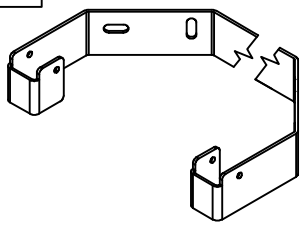
V1 V2



2x

E

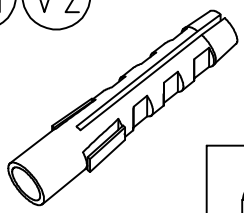
V3



2x

F

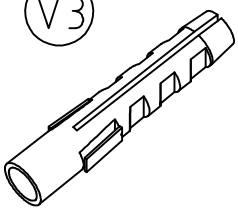
V1 V2



6x

G

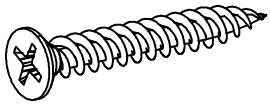
V3



8x

H

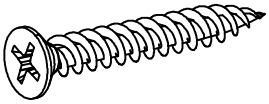
V1 V2



6x

I

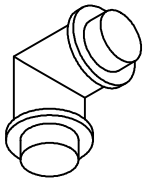
V3



8x

J

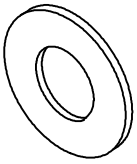
V1 V2 V3



2x

K

V1 V2 V3



1x

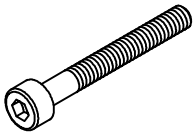
L

V1 V2 V3

1x

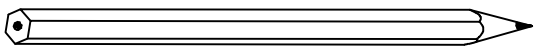
M

V1 V3

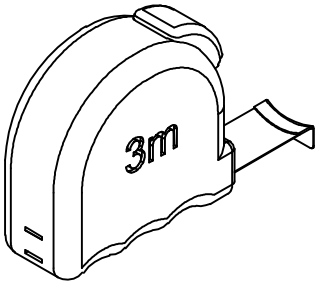


2x

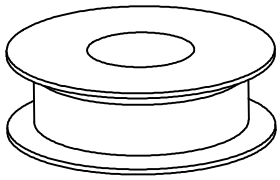
N



O

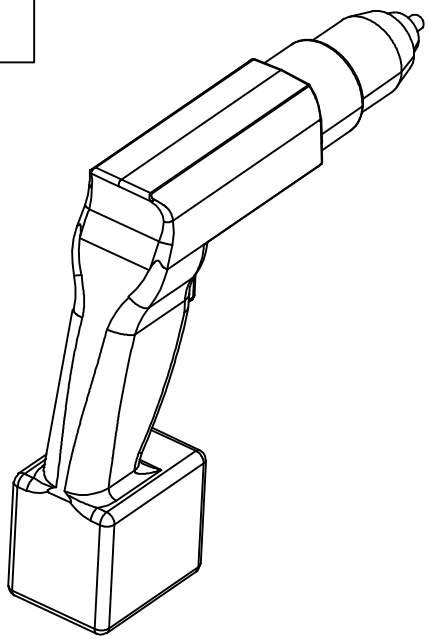


P



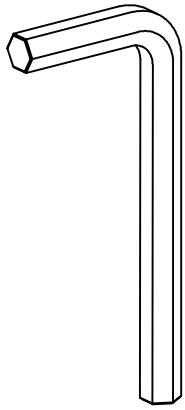
TEFLON

Q



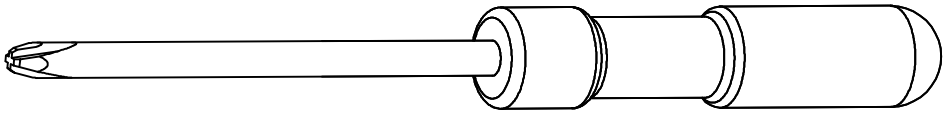
R

S

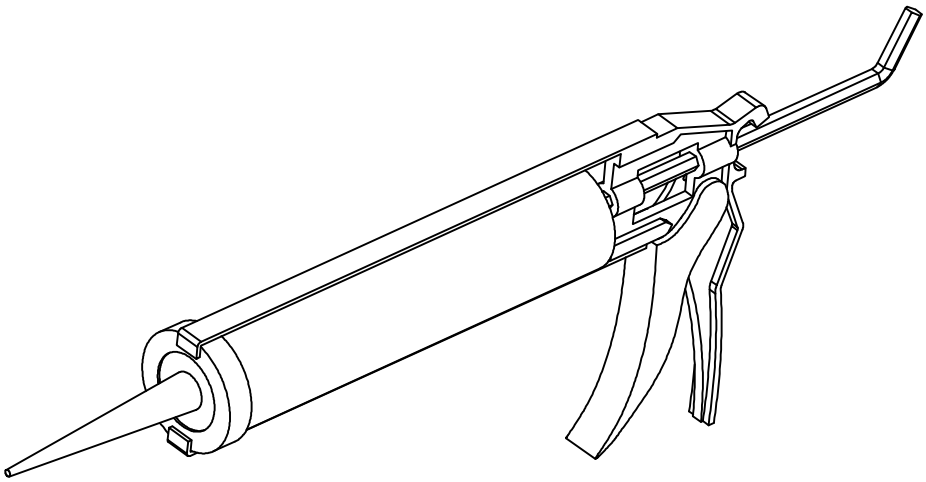


IMBUS 2.5

T

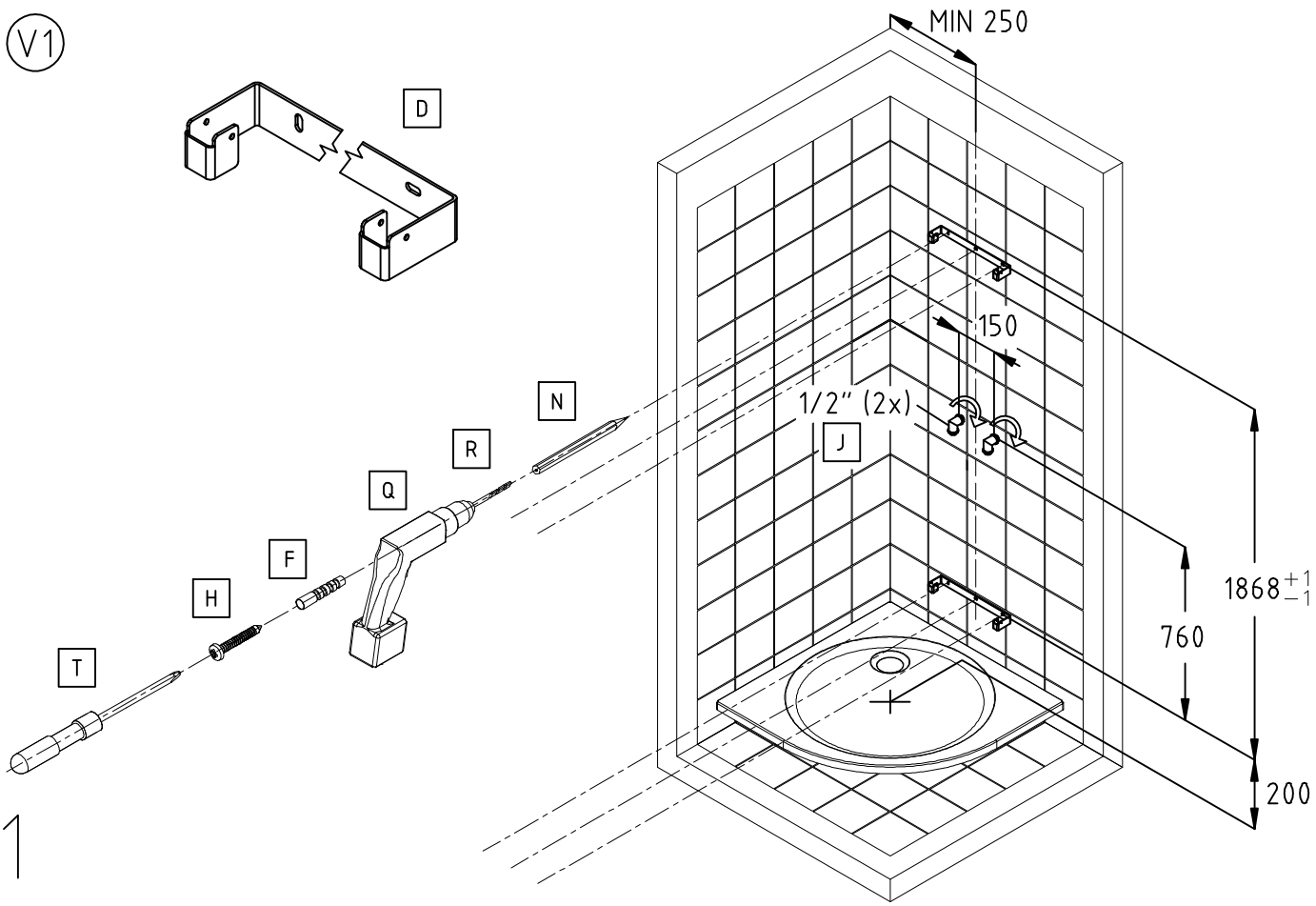


U



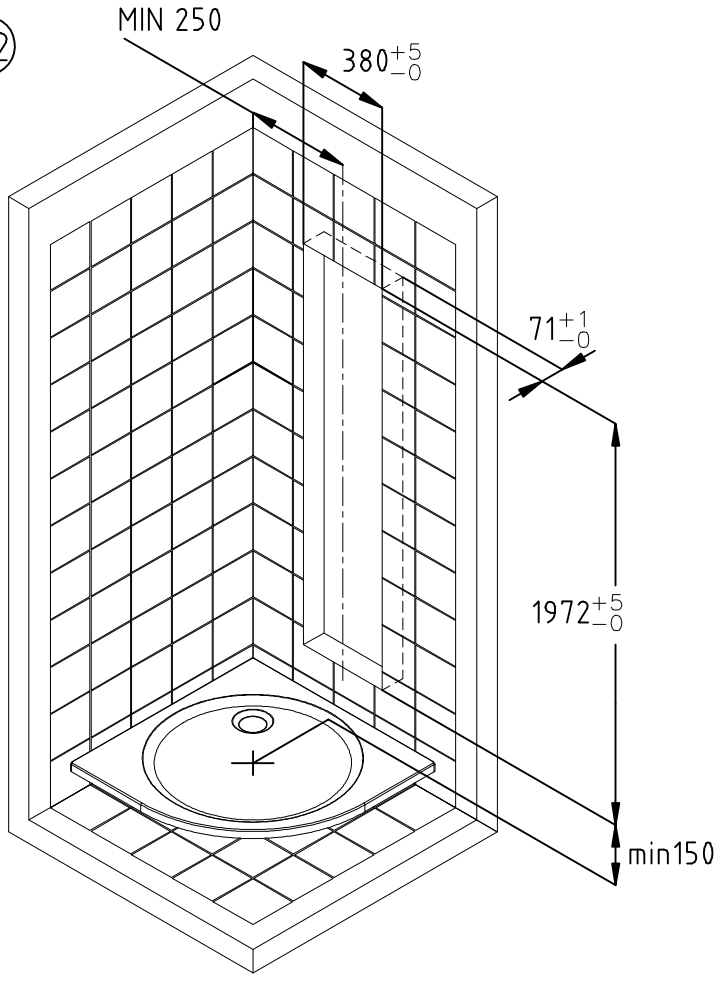
SILIKON

V1


D
N
R
Q
F
H
T
MIN 250
150
1/2" (2x)
J
1868 +1 −1
760
200

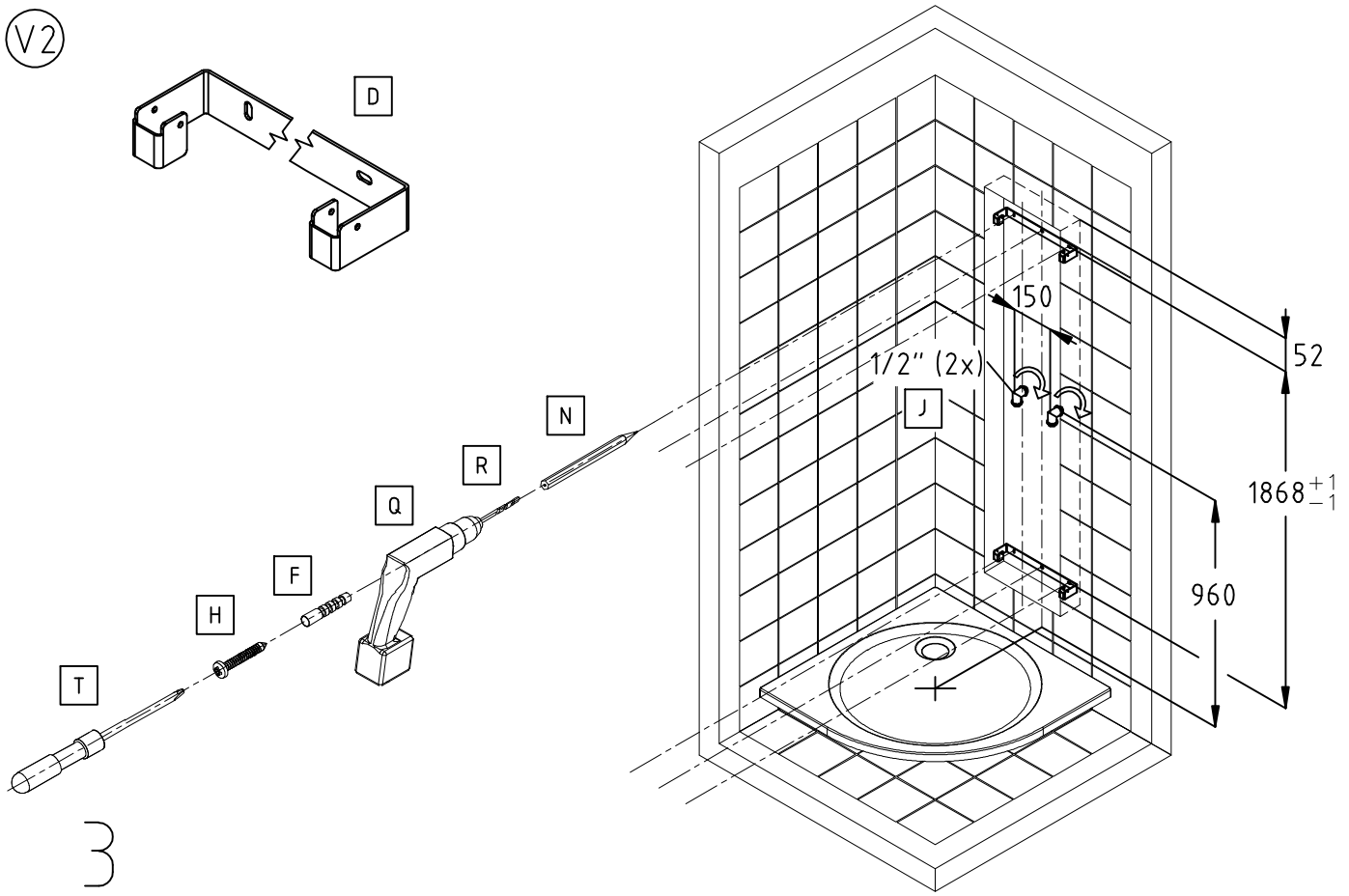
1

V2


MIN 250
380 +5 −0
71 +1 −0
1972 +5 −0
min150

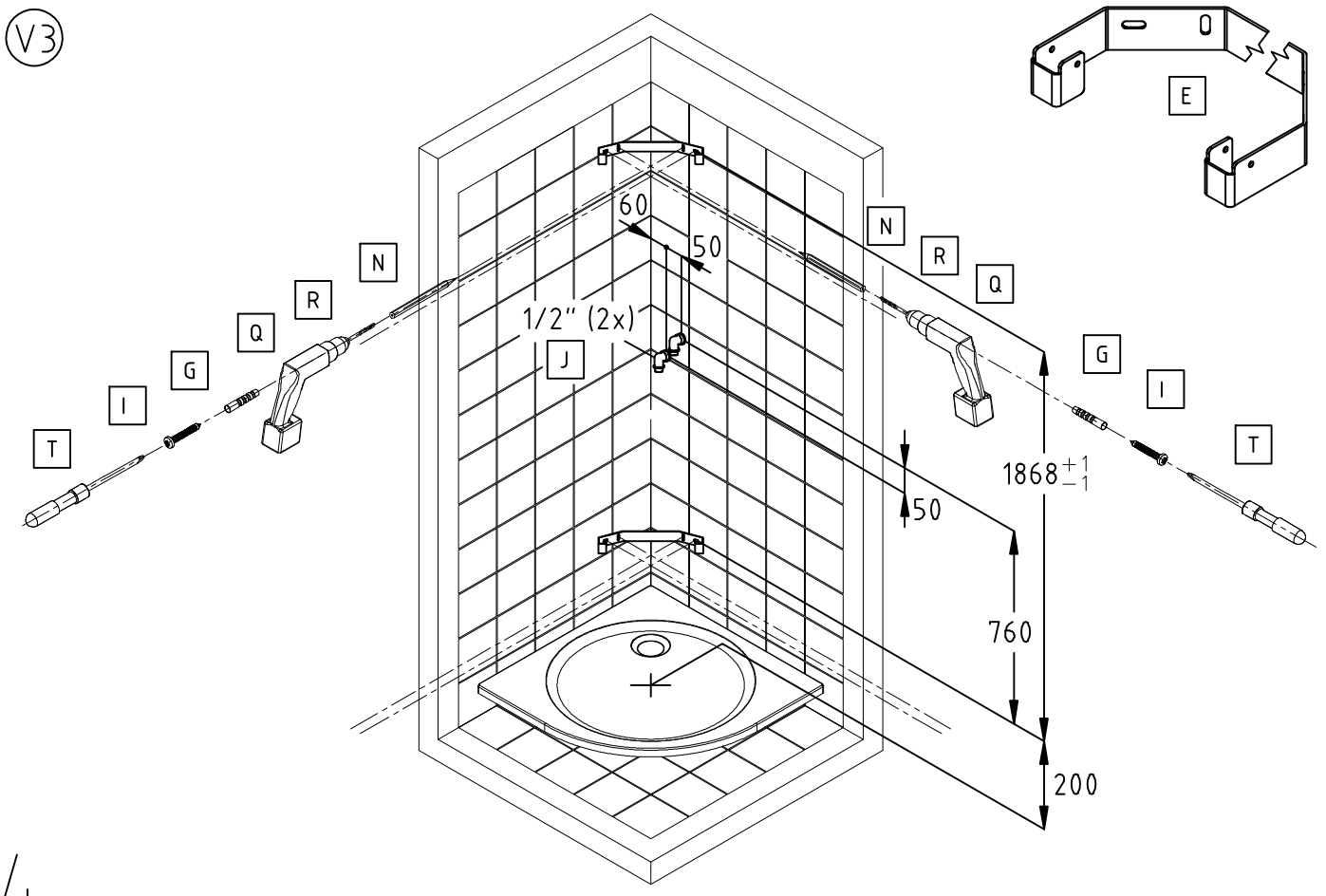
2

V2


D
N
R
Q
F
H
T
150
52
1/2" (2x)
J
1868 +1 −1
960

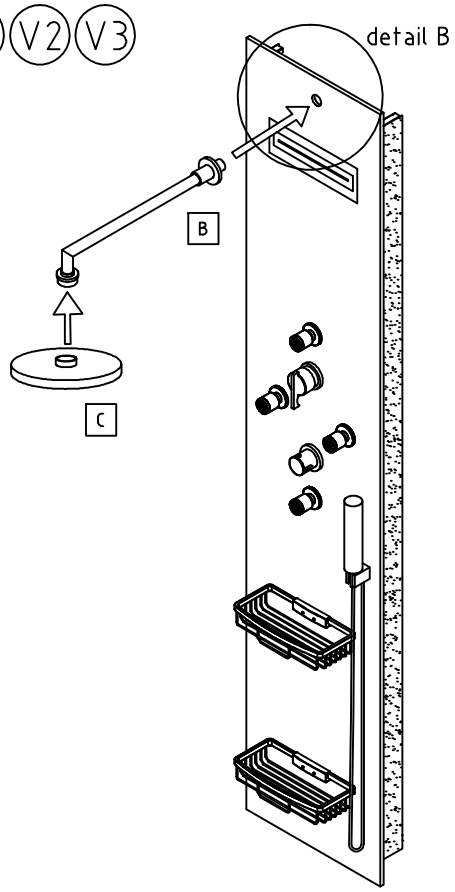
3

V3


E
60
50
N
R
Q
1/2" (2x)
J
G
I
T
1868 +1 −1
50
760
200

4

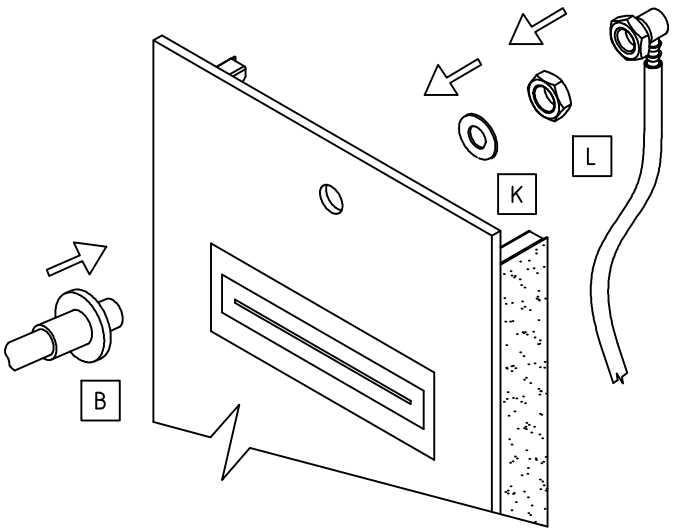
V1 V2 V3



5

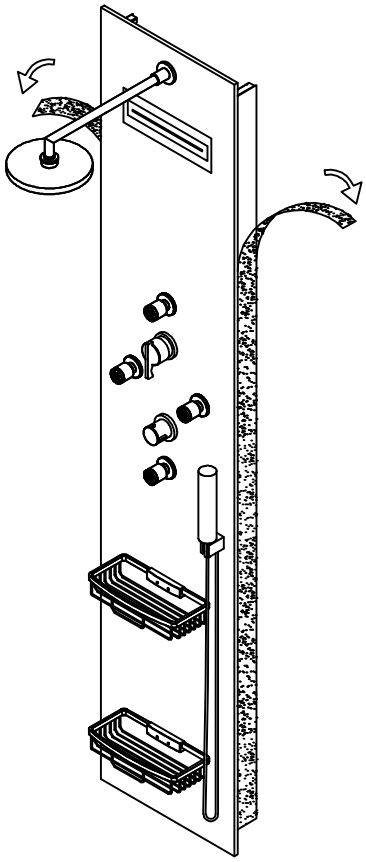
V1 V2 V3

detail B



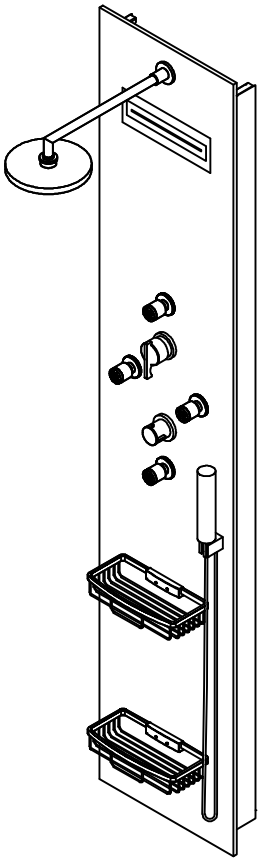
6

V1 V2 V3



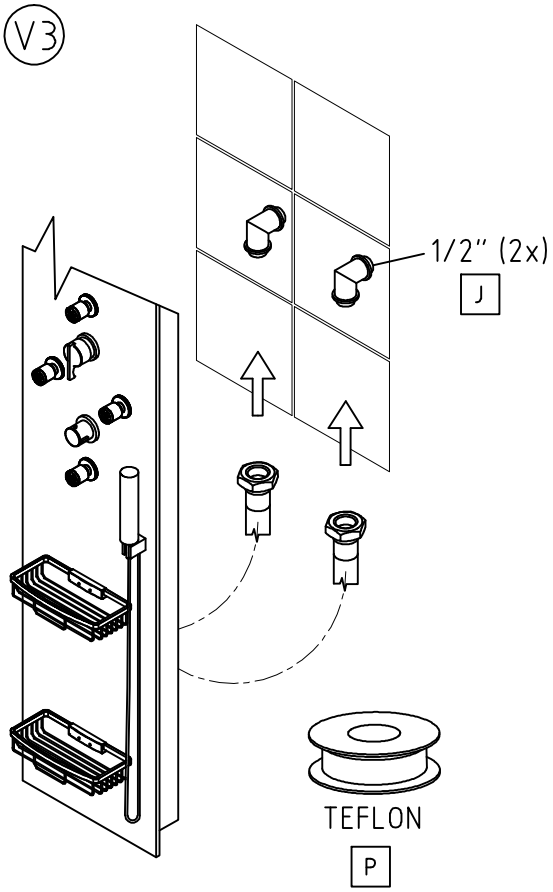
7

V1 V2 V3



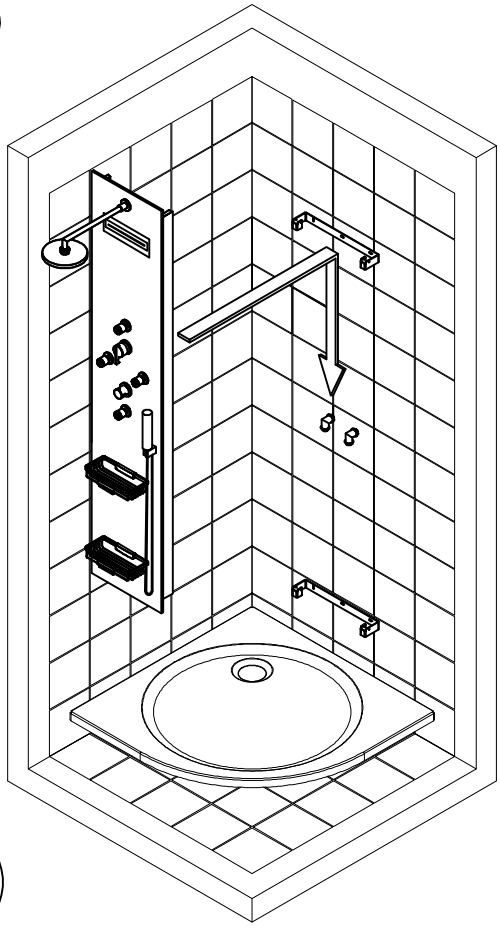
8

V1 V2 V3



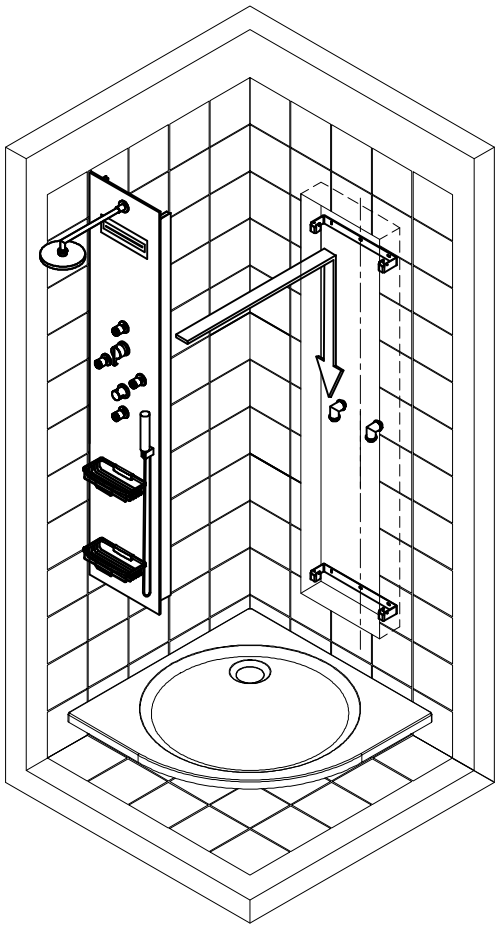
9

V1



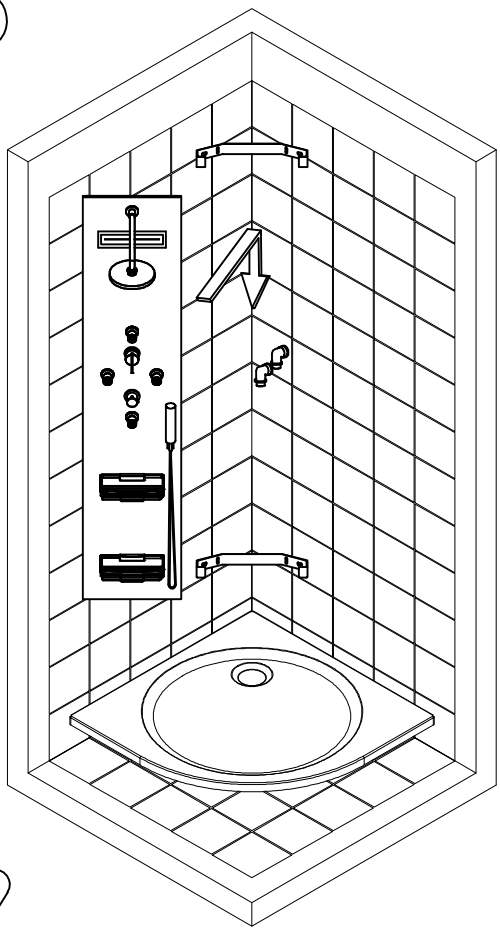
10

V2



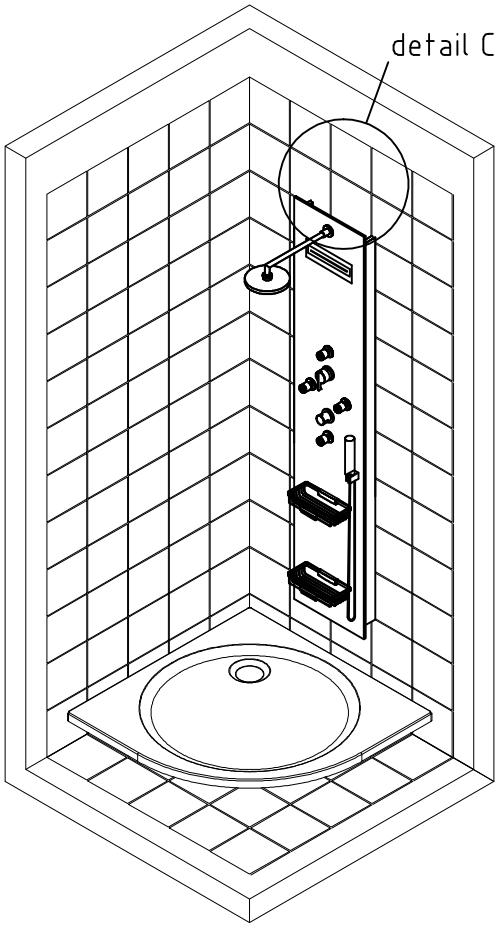
11

V3



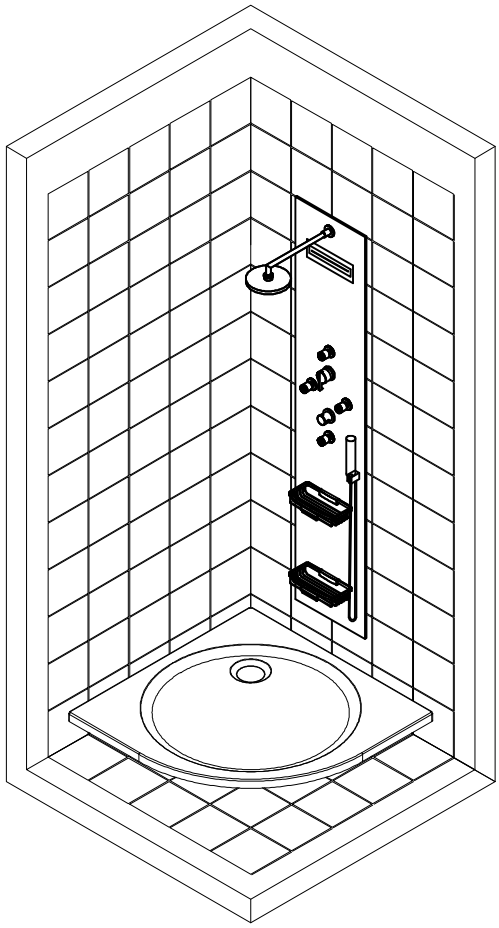
12

V1



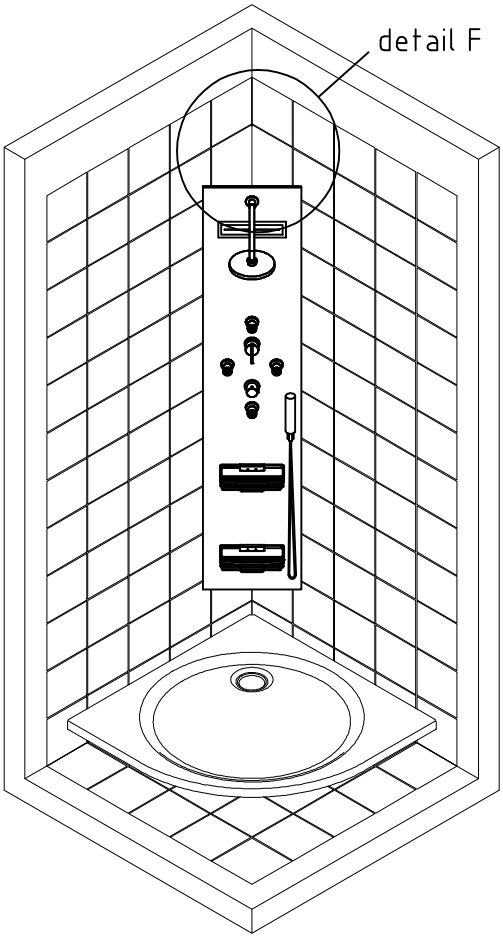
13

V2



14

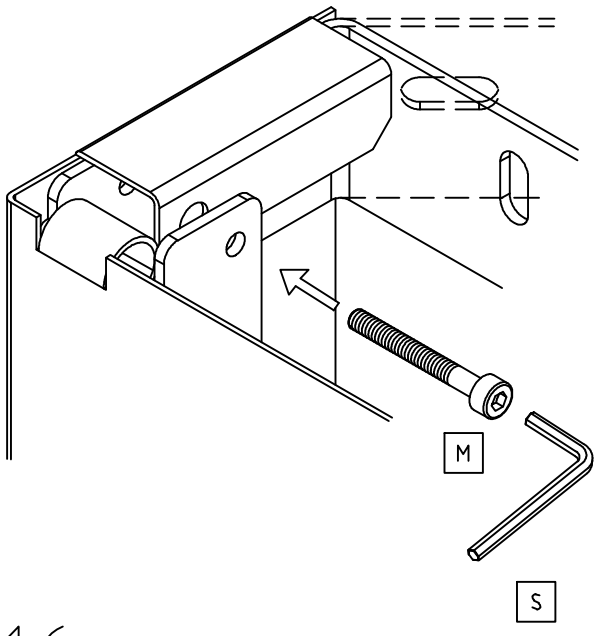
V3



15

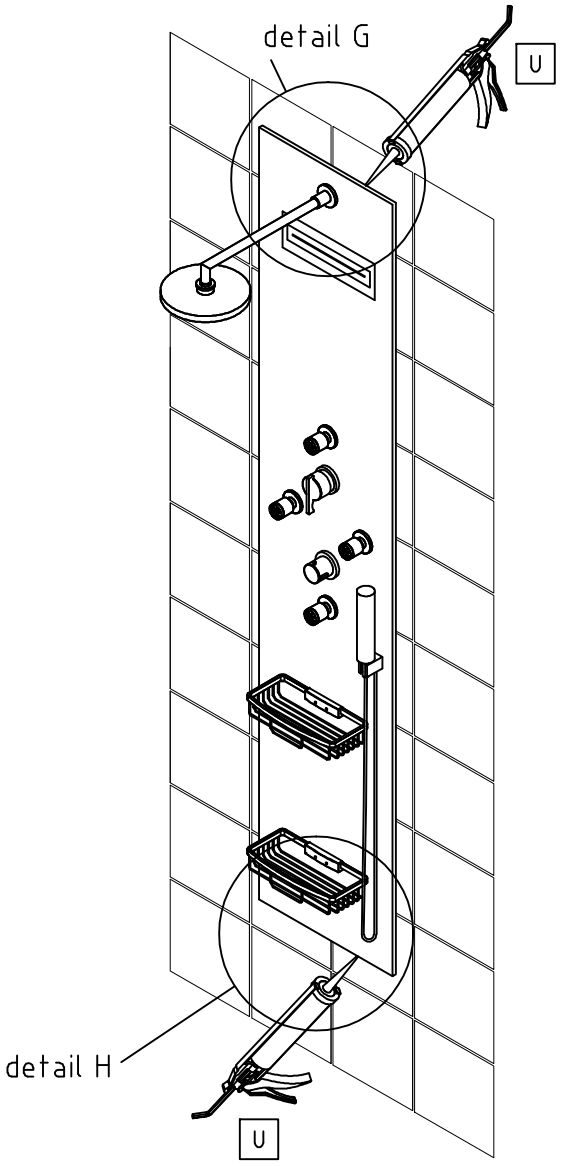
V1 detail C

V3 detail F



16

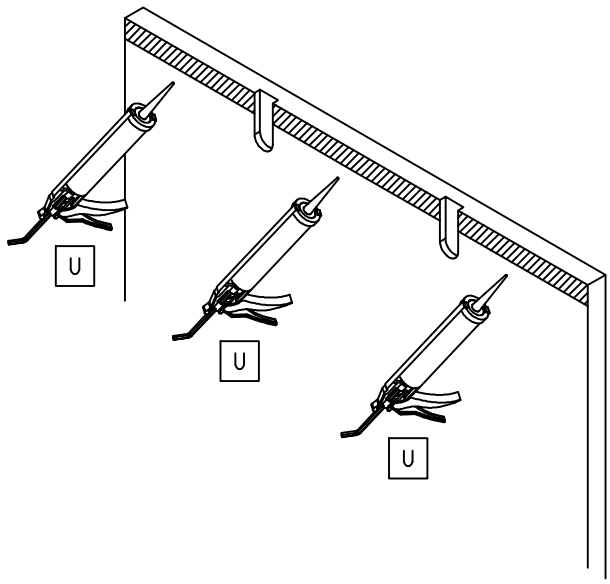
V2



17

V2

detail G
detail H



18