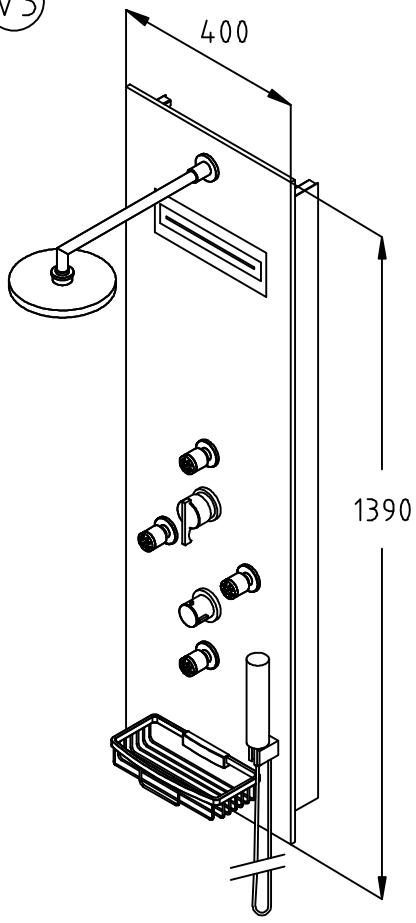
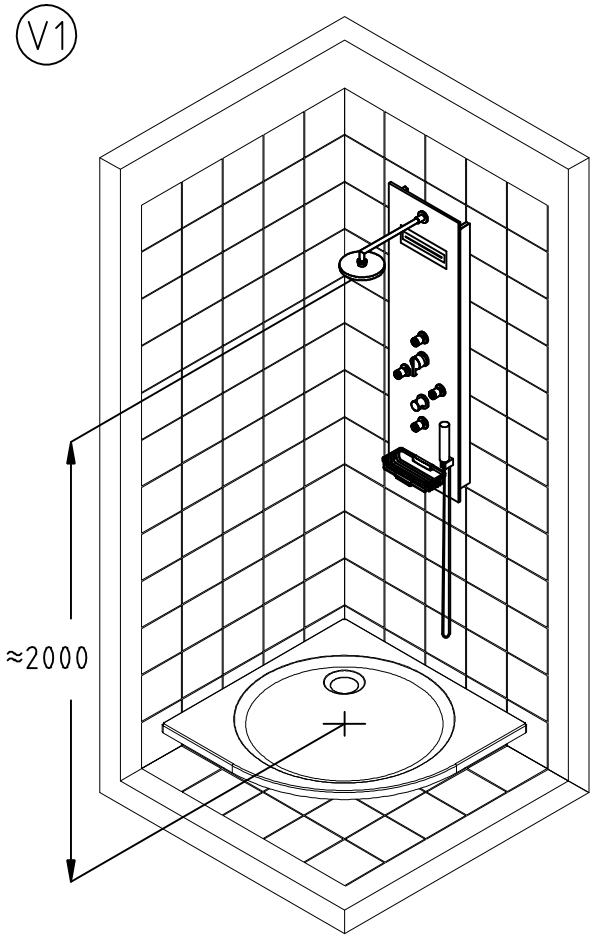
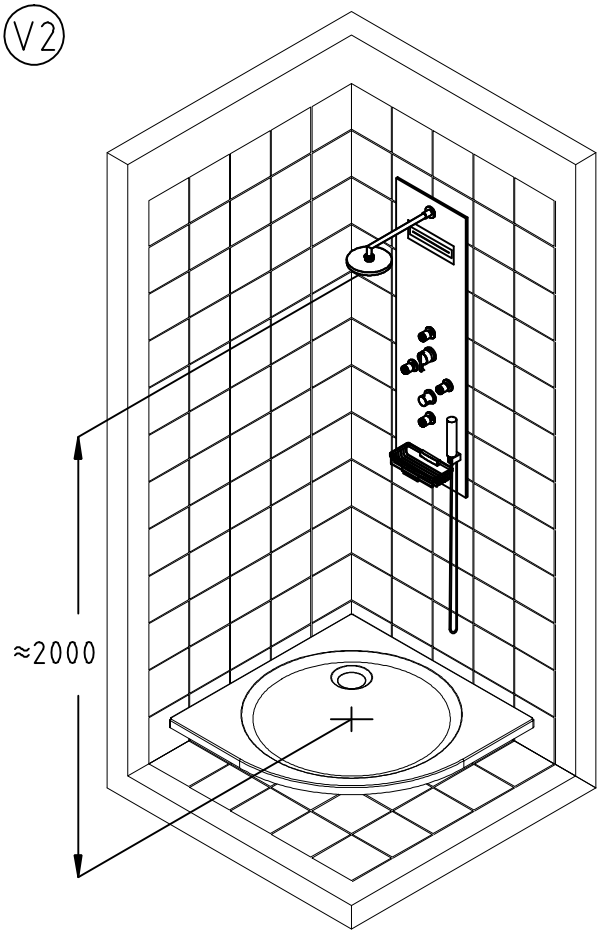
V1 V2 V3



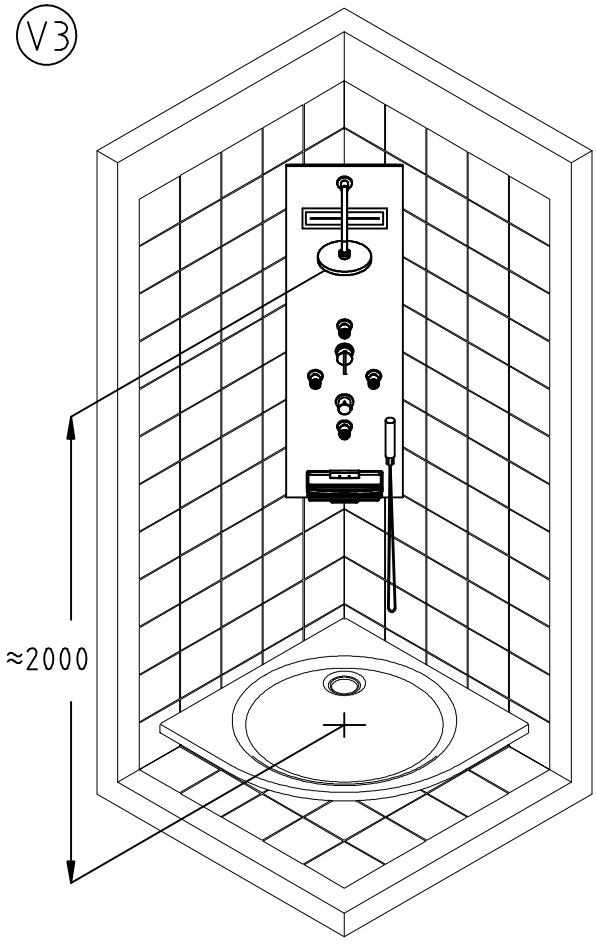
V1



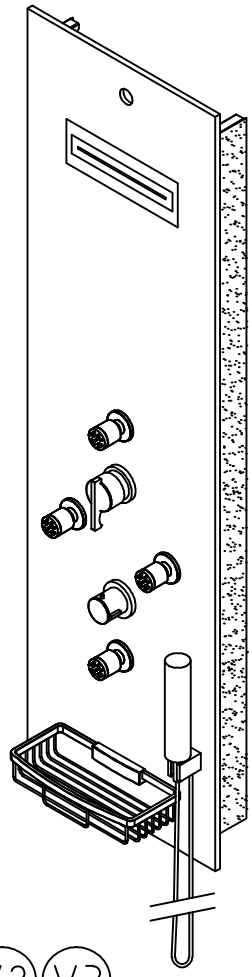
V2



V3



A

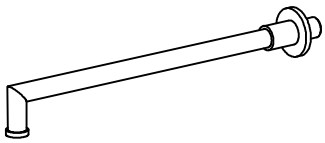


V1 V2 V3

1x

B

V1 V2 V3



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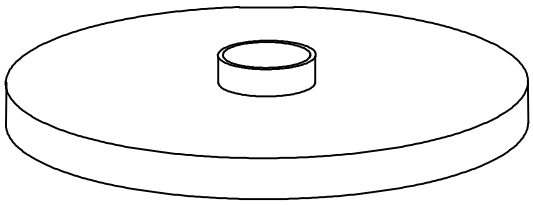
C

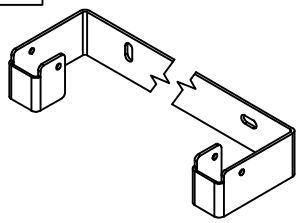
V1 V2 V3



1x

D

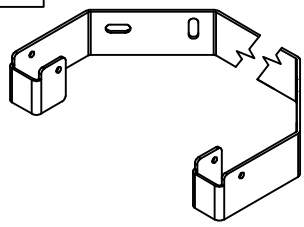
V1 V2



2x

E

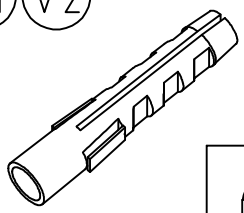
V3



2x

F

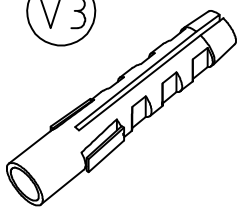
V1 V2



6x

G

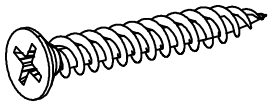
V3



8x

H

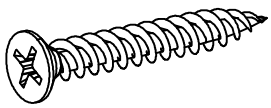
V1 V2



6x

I

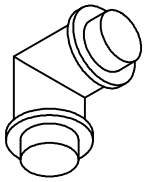
V3



8x

J

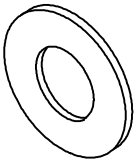
V1 V2 V3



2x

K

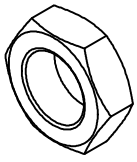
V1 V2 V3



1x

L

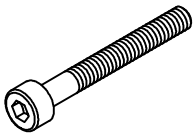
V1 V2 V3



1x

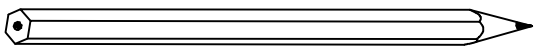
M

V1 V3



2x

N



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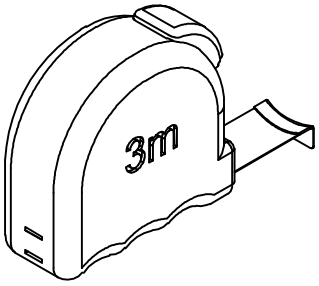
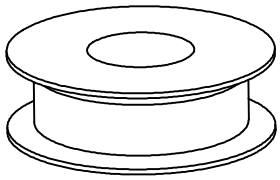
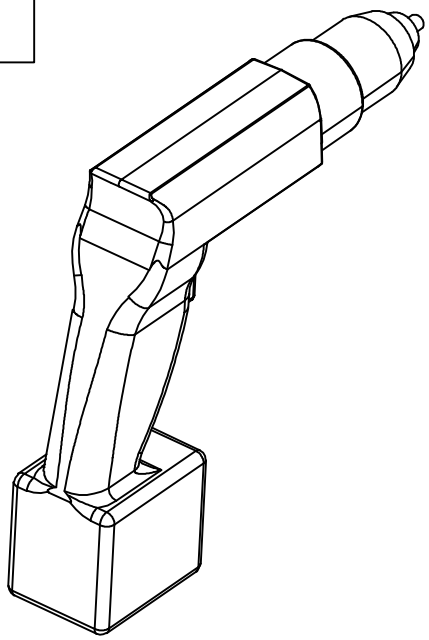


P



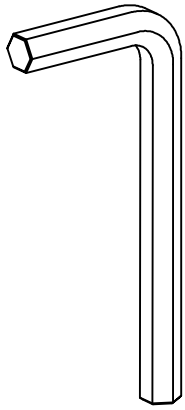
TEFLON

Q



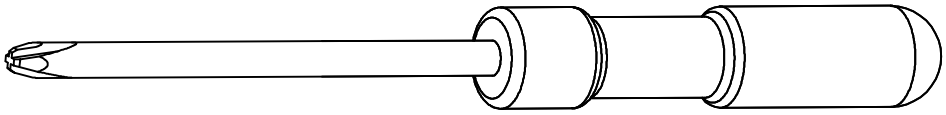
R

S



IMBUS 2.5

T



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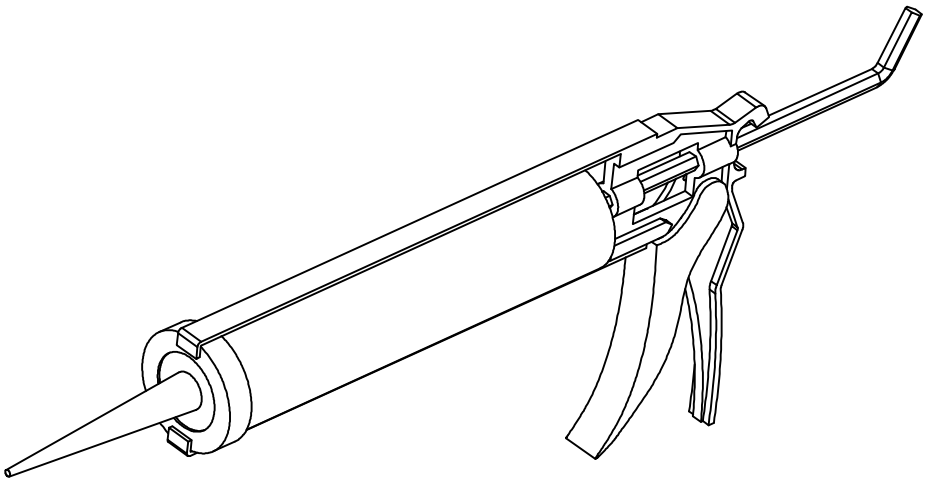
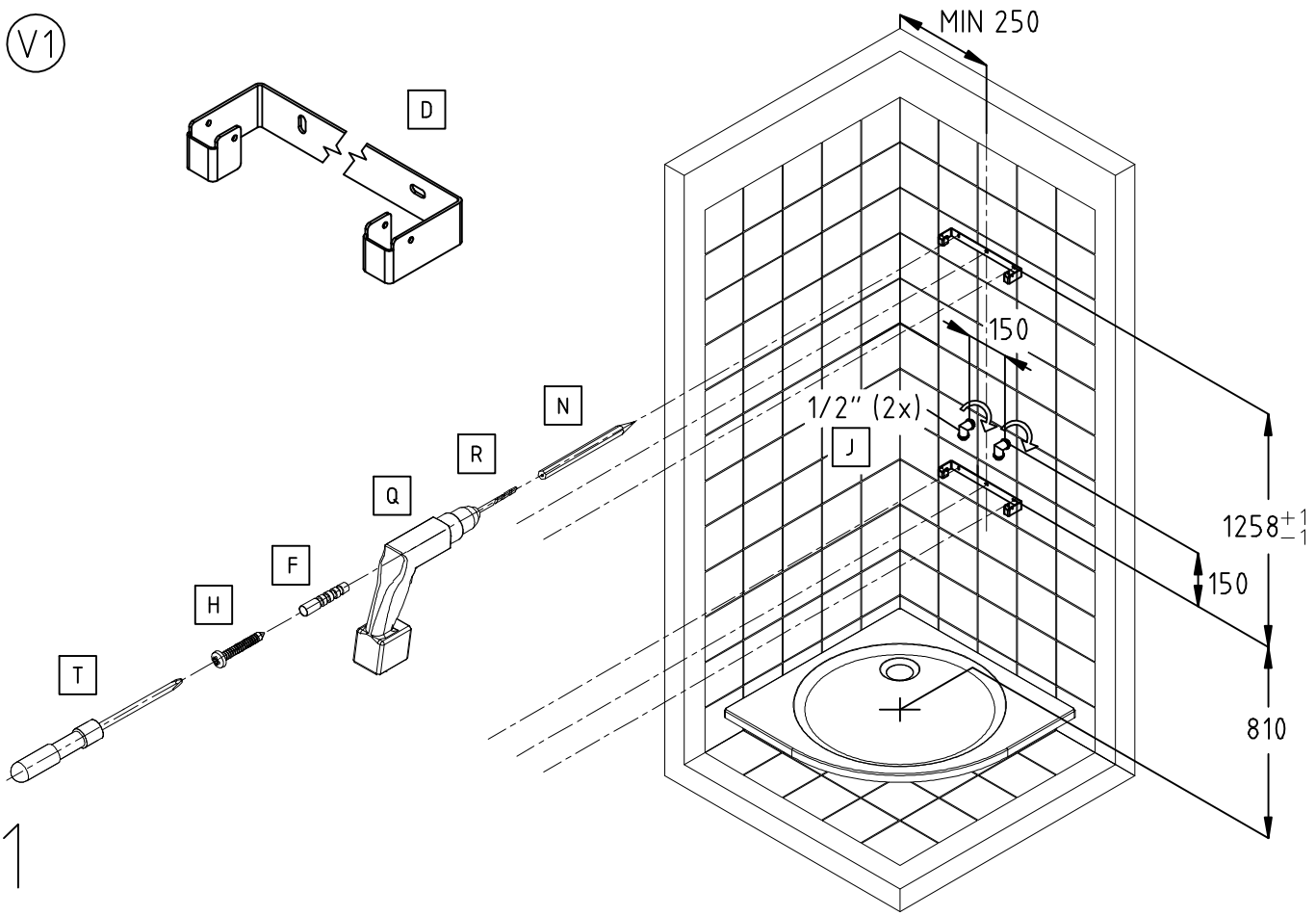


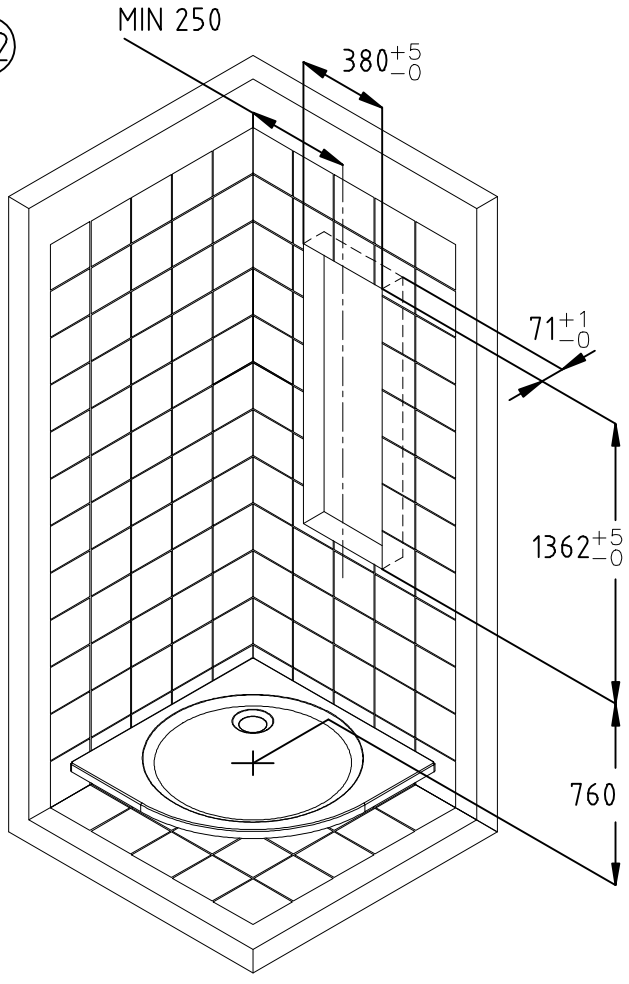
SILIKON

V1

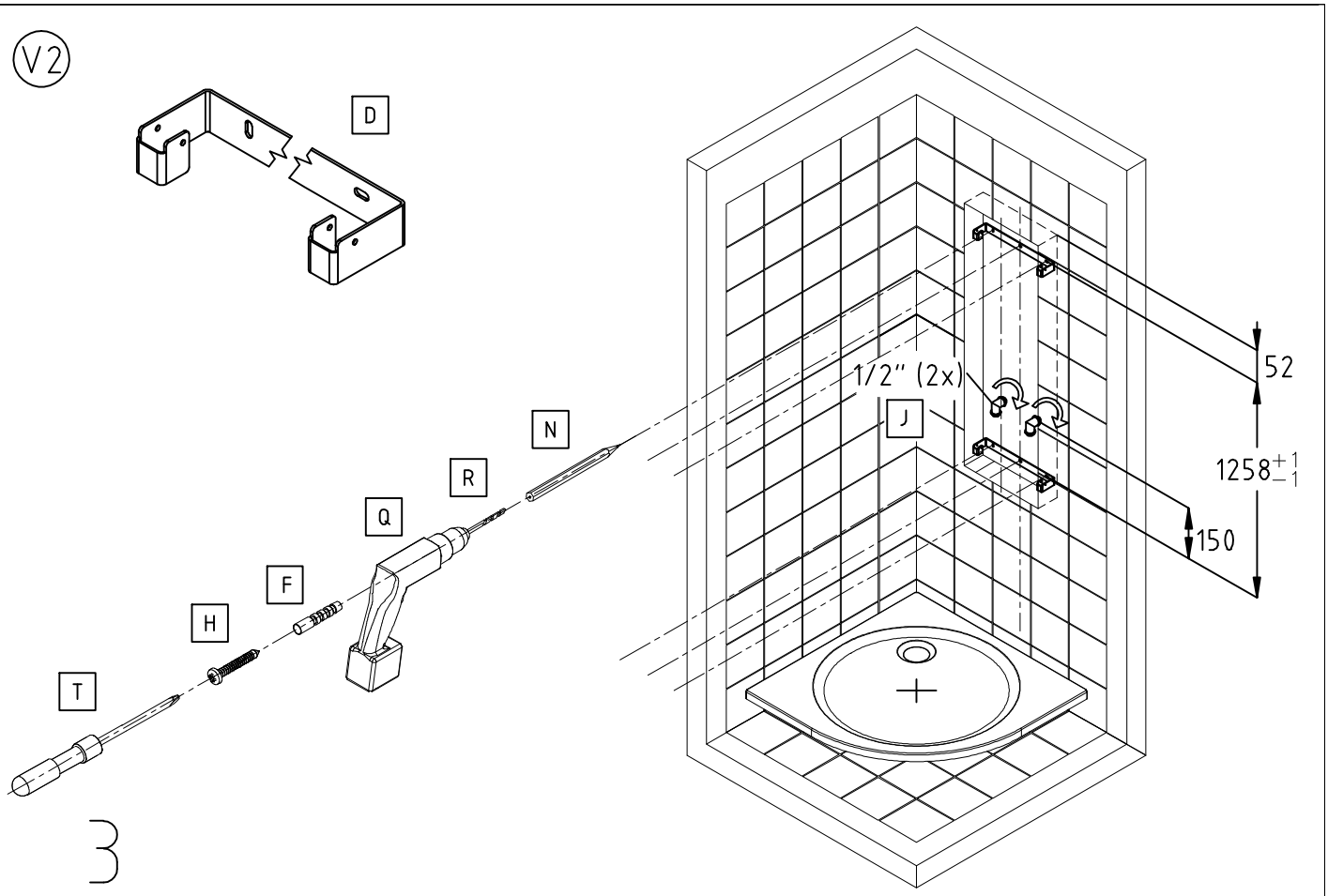

D
N
R
Q
F
H
T
MIN 250
150
1/2" (2x)
J
1258+1 −1
150
810

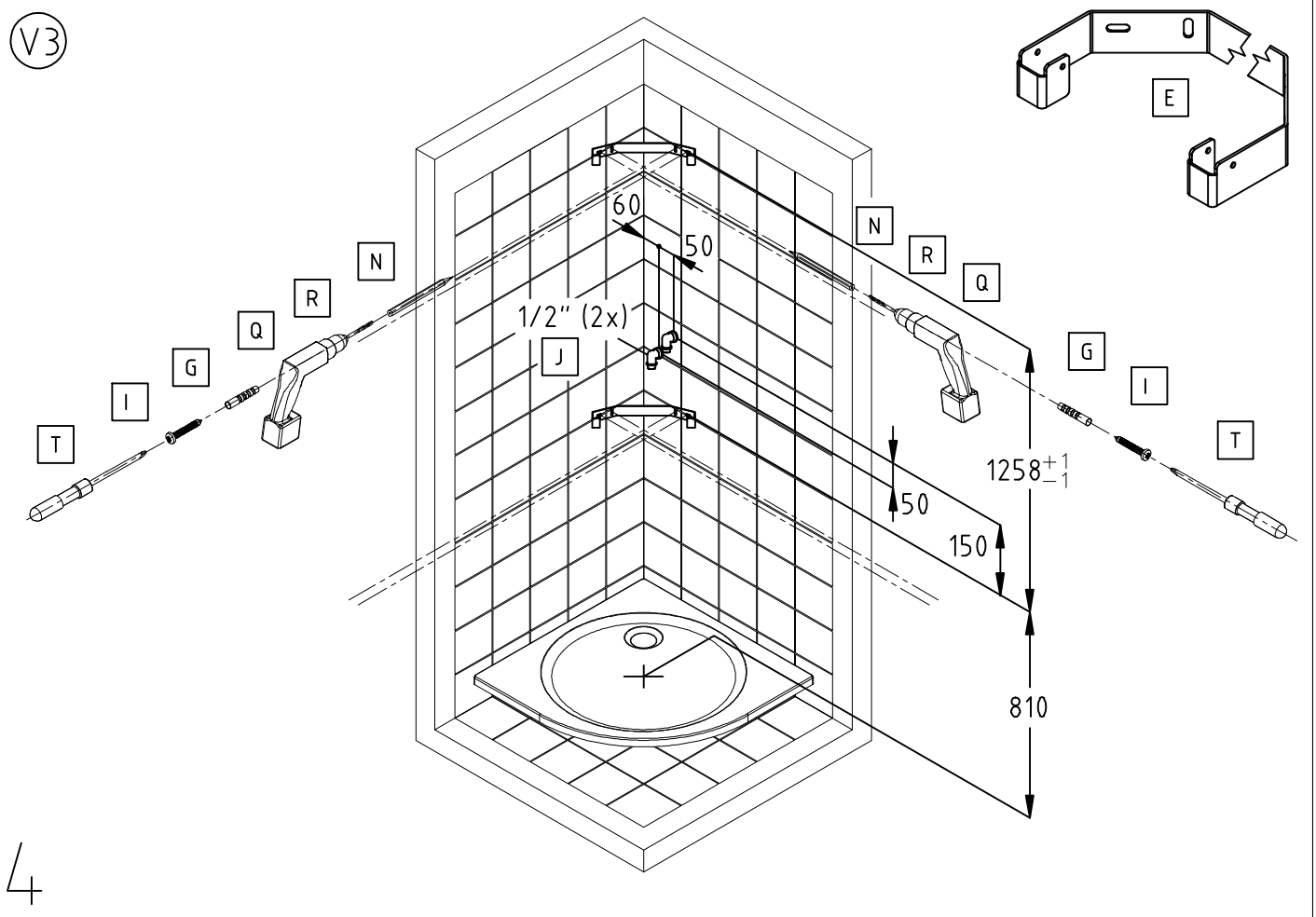
1

V2

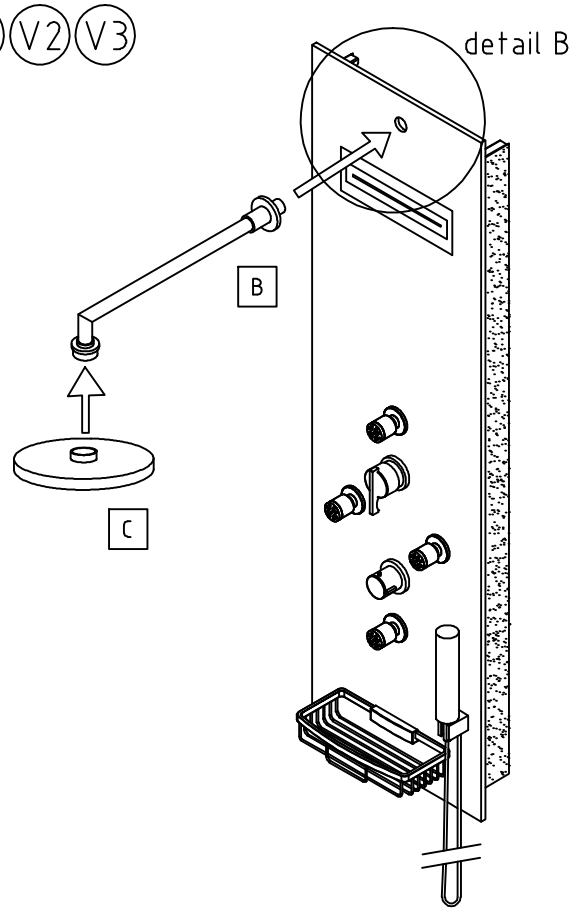

MIN 250
380+5 −0
71+1 −0
1362+5 −0
760

2


V2
D
1/2" (2x)
J
52
1258+1 -1
150
N
R
Q
F
H
T
3


V3
E
60
50
1/2" (2x)
J
N
R
Q
G
I
T
50
150
1258+1 -1
810
4

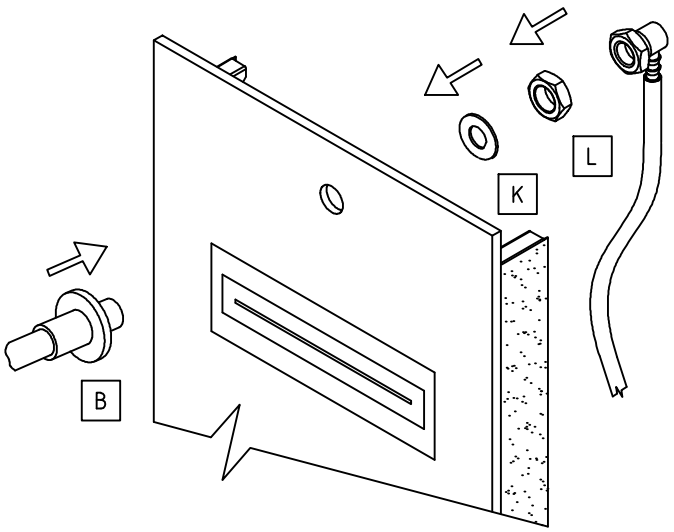
V1 V2 V3



5

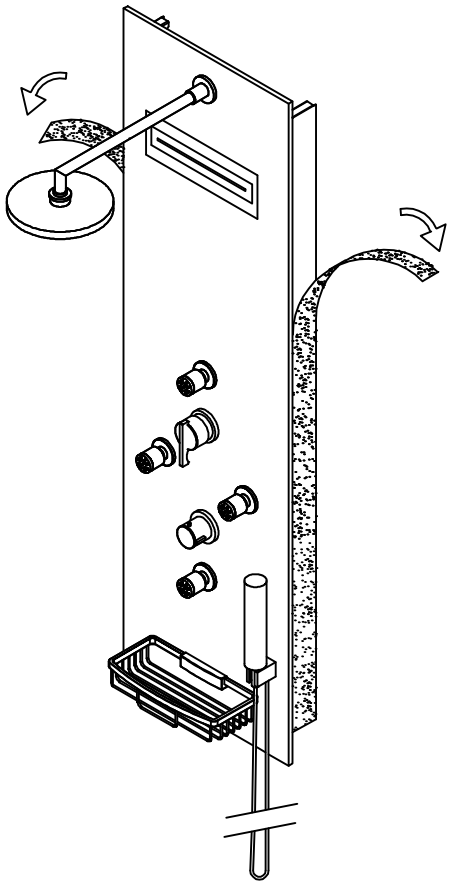
V1 V2 V3

detail B



6

V1 V2 V3



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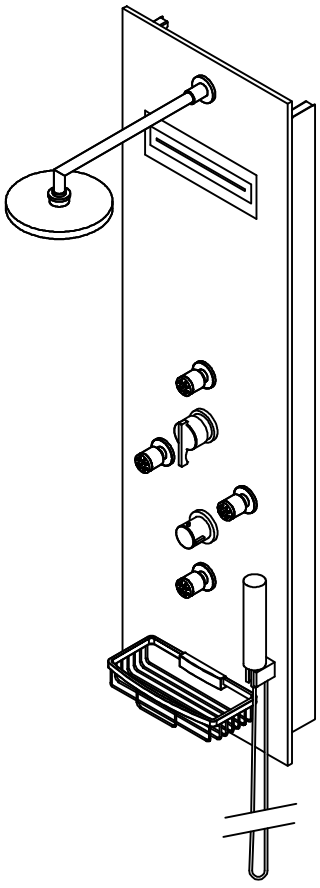
V1 V2 V3



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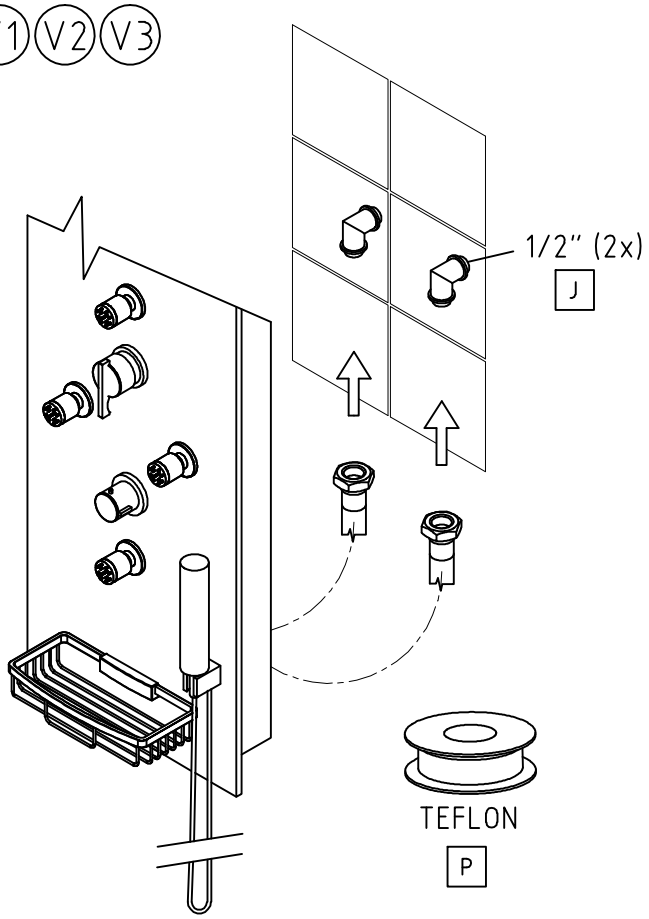
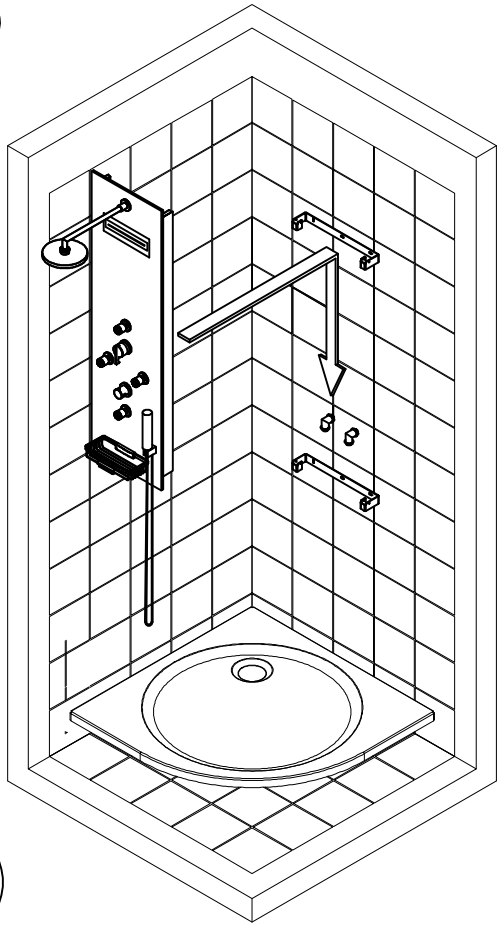
V1 V2 V3



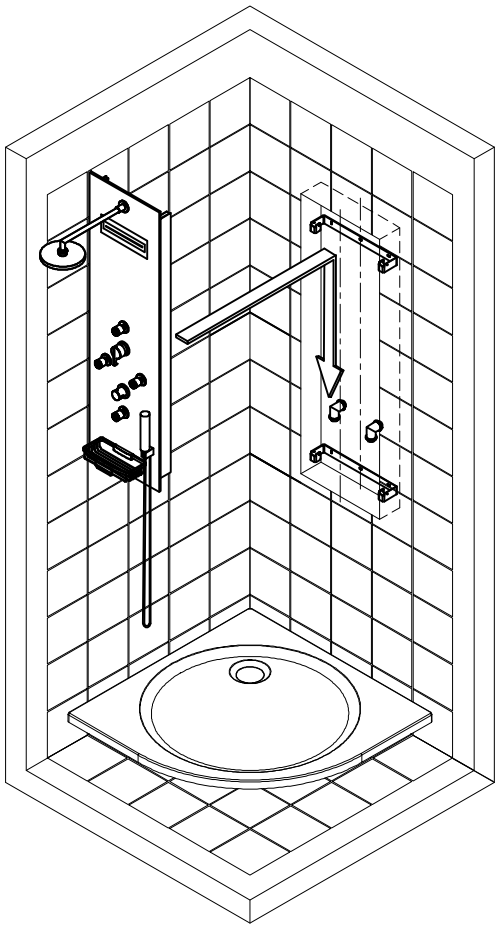
9

V1



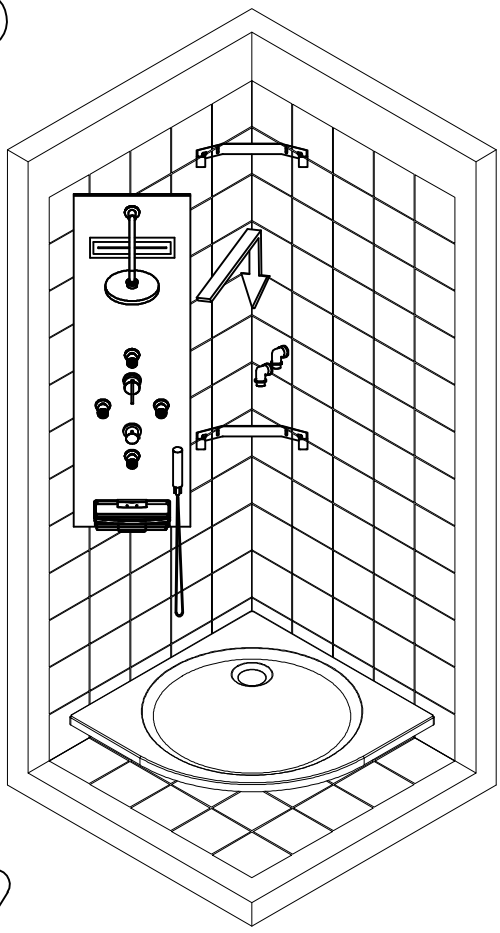
10

V2



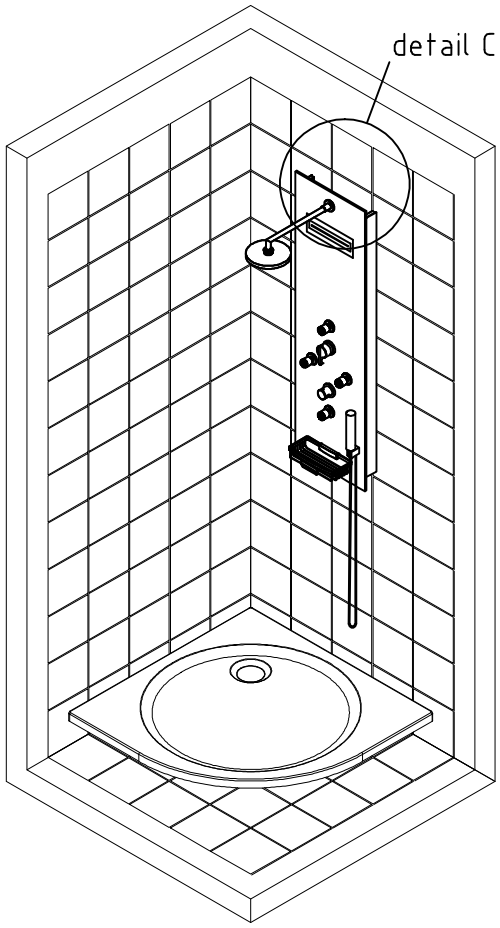
11

V3



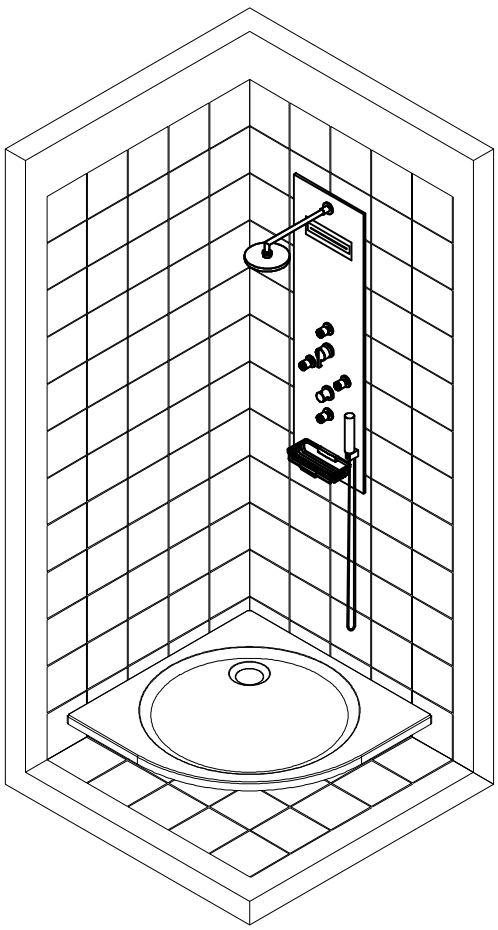
12

V1



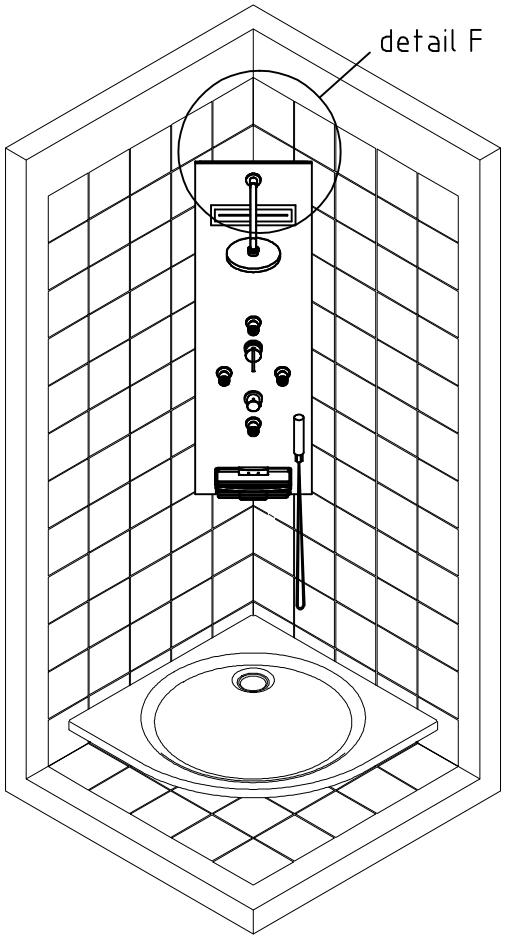
13

V2



14

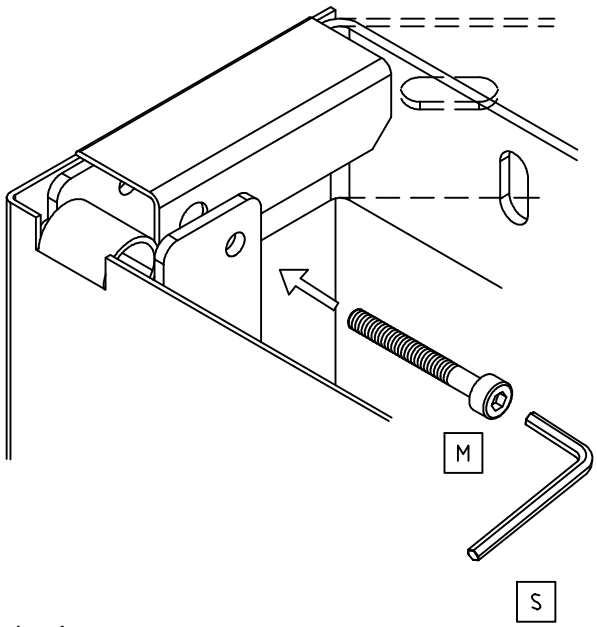
V3



15

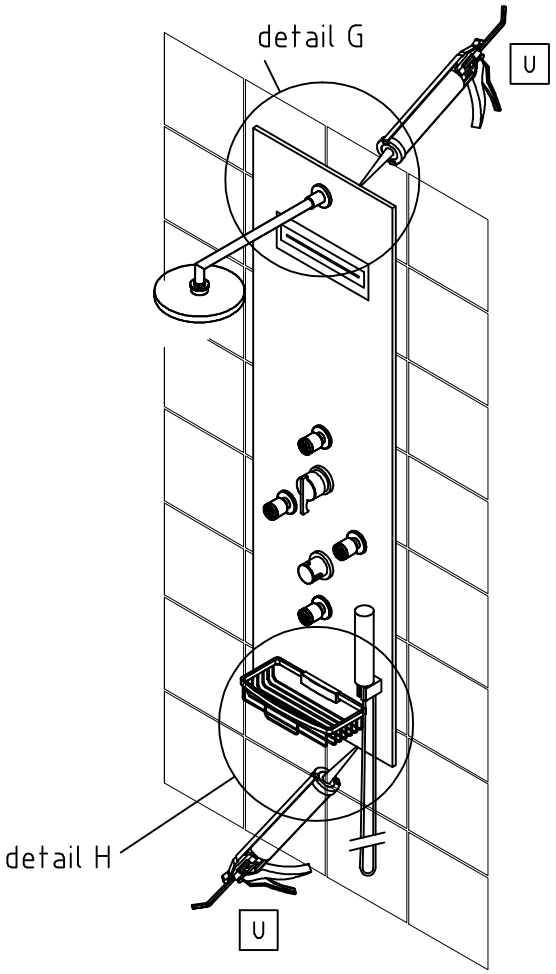
V1 detail C

V3 detail F



16

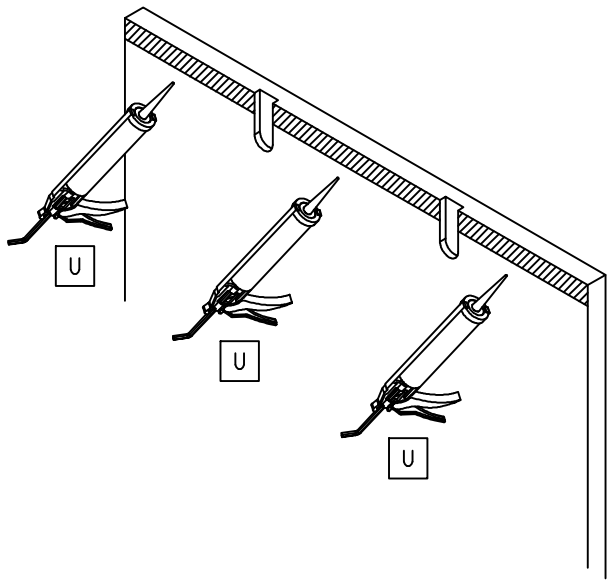
V2



17

V2

detail G
detail H



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